AN INTEGRATED, LOSSLESS, AND ACCURATE CURRENT-SENSING TECHNIQUE FOR HIGH-PERFORMANCE SWITCHING REGULATORS

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AN INTEGRATED, LOSSLESS, AND ACCURATE CURRENT-SENSING TECHNIQUE FOR HIGH-PERFORMANCE SWITCHING REGULATORS

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TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF SYMBOLS AND ABBREVIATIONS

I_L	Inductor Current
ΔI_L	Inductor Ripple Current
i_L	Small-Signal Changes of Inductor Current
I_{Load}	DC-DC Converter Load Current
D	Duty Cycle
d	Small-Signal Changes of Duty Cycle
L	Inductor Value
M_1	Inductor Current Ramp-Up Slope
M_2	Inductor Current Ramp-Down Slope
M_c	Compensation Current Ramp Slope
R_{ESR}	Inductor ESR
R_{C_ESR}	Output Capacitor ESR
V_{Sense}	Output Voltage of Current-Sensing Circuit
R_{Sense}	Current-Sensing Circuit Gain (V/A)
V_{DD}	Supply Voltage
V_{os}	Offset Voltage
Q(e)	Quantization Error
V_{Ph}	Switching node (phase node) of a DC-DC converter
ICMR	Input Common-Mode Range
PSRR	Power Supply Rejection Ratio
CMRR	Common Mode Rejection Ration
CCM	Continuous-Conduction Mode
DCM	Discontinuous-Conduction Mode
ESR	Equivalent Series Resistance
PWM	Pulse Width Modulation
PTAT	Proportional To Absolute Temperature

SUMMARY

Switching power converters are an indispensable part of every battery-operated consumer electronic product, nourishing regulated voltages to various subsystems. In these circuits, sensing the inductor current is not only necessary for protection and control but also is critical to be done in a lossless and accurate fashion for state-of-the-art advanced control techniques, which are devised to optimize transient response, increase the efficiency over a wide range of loads, eliminate off-chip compensation networks, and integrate the power inductor. However, unavailability of a universal, integrable, lossless, and accurate current-sensing technique impedes the realization of those advanced techniques and limit their applications. Unfortunately, use of a conventional series sense resistor is not recommended in high-performance, high-power switching regulators where more than 90% efficiency is required because of their high current levels (e.g., in the order of amperes) resulting in unacceptable power losses in the sense resistor, which severely reduce the overall power efficiency of the system (e.g., by 2-10%). A handful of lossless current-sensing techniques are available but their accuracies are significantly lower than the traditional sense resistor scheme.

Among available lossless but not accurate techniques, an off-chip, filter-based method that uses a tuned filter across the inductor to estimate current flow and its accuracy is dependent on the inductance and its equivalent series resistance (ESR) was selected for improvement because of its inherent continuous and low-noise operation. A schemes is proposed to adapt the filter technique for integration by automatically adjusting bandwidth and gain of an on-chip programmable g_m-C filter to the off-chip power inductor during the system start-up through measuring the inductance and its ESR. In the start-up, first during a tuning phase, a triangular test signal is forced into the inductor and the filter high-frequency gain is varied until the gain-bandwidth is adjusted to the target value. Then, during a calibration phase, a DC test signal is forced into the inductor and the filter DC gain is varied until targeted DC gain is resulted. After tuning and calibration phases are finished, the filter is set to accurately measure the inductor current during the normal operation of the switching regulator.

To verify the proposed technique, an integrated circuit (IC) prototype in AMI's 0.5-μm CMOS process was developed, designed, implemented, and evaluated. The final

chip included a low-offset continuous, programmable gain and bandwidth g_m-C filter, tuning and calibration circuits to adjust the filter during startup, and current generator to force test current into the inductor at startup. A current-mode controlled buck DC-DC, designed to meet specifications of Lithium-Ion-battery-supplied portable applications, was also implemented as a test bed for the proposed current-sensing circuit.

The IC prototype achieved overall DC and AC gain errors of 8% and 9%, respectively, at 0.8 A DC load and 0.2 A ripple currents for inductors from 3.5 μH-14 μH and ESR from 48 mΩ to 384 mΩ when lossless, state-of-the-art schemes achieve 20–40% error and only when the nominal specifications of power component (power MOSFET or inductor) are known. Moreover, the proposed circuit improved the efficiency of a test bed current-mode controlled switching regulator by more than 2.6% compared to the traditional sense resistor technique with a 50 mΩ sense resistor.

CHAPTER 1

INTRODUCTION

The demand for high-performance, portable electronic devices, such as laptops, cellular phones, and digital cameras, continues to grow and expand at an unrelenting pace. As portable devices include more functions, their energy needs increase. With portable devices, from a power-management perspective, the design objective is to extend battery life, that is, increase the total time that a battery operates before it is recharged, as much as possible without increasing battery size and weight. Usually, this goal can be achieved either by building better batteries or lowering the power requirements of the system.

Micro generators implemented in micro electro-mechanical systems (MEMS) technologies [1], fuel cells [2], and nuclear batteries [3] have potentially more energy density compared to traditional Lithium Ion (Li-Ion) and Nickel Cadmium (NiCd) batteries and are candidates for energy sources of future portable devices. Other researchers have also proposed energy harvesters to acquire energy from the devices' surrounding environment to recharge the batteries and provide the needs of the system, virtually providing an inexhaustible source of energy [4].

Many circuit- and system-level strategies have been designed to lower the power consumption of electronic systems. For example, efficient coding schemes can result in lower power-consuming transceivers [5], adaptive power-tracking techniques increase the efficiency of power amplifiers [6], and biasing transistors in weak inversion [7] results in lower power analog electronics.

However, another power loss occurs in electronic systems when battery power is distributed among subsystems. In today's high-performance devices, each subsystem often requires a specific supply voltage level, whereas only one voltage level is available at the battery output. For example, in a cellular phone, analog/RF, digital, and liquid crystal display (LCD) subsystems require independent voltage supplies; a state-of-the-art digital camera usually needs about 15 different supply source voltages. Therefore, the

battery voltage is conditioned and converted to all required voltage levels using power-efficient voltage regulators.

There are three major categories of DC voltage regulators: charge pumps, linear regulators, and switching converters (i.e., DC-DC converters). Charge pumps convert the input voltages to a higher voltage levels, but their operation is limited to relatively low power levels. Linear regulators only convert higher voltage levels to lower voltage levels, and their efficiency, which is approximately the ratio of the output voltage to the supply voltage, can be relatively low. Switching regulators, which benefit from the energy-storing capacities of large inductors and capacitors, convert battery voltages efficiently to both lower and higher voltage levels. Because of their switching nature, the output voltage of DC-DC converters experiences more ripples; therefore linear regulators are the designer's choice for providing power to noise-sensitive blocks like low-jitter phase-locked loops. Basic switching regulator circuits have efficiencies of more than 80% for a specific load current range. To squeeze all power available out of the battery efficiently, high-performance switching regulators are designed to achieve efficiencies of more than 95% for full load-current. Efficiently and accurately the internal states of the regulator allows converters to adapt to various operating conditions for optimum efficiency and transient response.

1.1. Current Sensing in Switching Regulators

Current-sensing circuits are one of the more critical building blocks used for control and protection of DC-DC converters [8-9]. Every switching regulator includes an over-current detection circuit, which protects the system against over-current events. Furthermore, the sensed inductor current is a rich source of information for the operating state of the system. This information source is exploited in current-mode controllers, especially in multi-phase converters, and a growing number of dynamically adaptive supplies where the operating region is dependant on the load current for enhanced power-efficiency performance.

Unfortunately, the conventional and simple series sense resistor incurs unacceptable power losses. Since current flow in DC-DC converters is high (i.e., on the order of amperes), even small resistors cause significant losses, severely reducing the

overall power efficiency of the system (by as much as 2% to 10%). Reducing the series resistance (e.g., 1 mΩ for 1 A) is prohibitive because the detected signal is overwhelmed by noise and offsets (i.e., accuracy is poor), which is why the series resistor technique is unacceptable in today's high-performance converters, like those used in portable applications where more than 90% efficiency is required over the entire load-current range [10].

A handful of lossless current-sensing techniques are available, but their accuracies are significantly lower than the traditional sense resistor scheme [10]. The MOSFET R_{on} [11], current-sensing FET (sense-FET) [11-17], and filter [11, 18] schemes are among the more popular techniques (Table 1.1). The MOSFET R_{on} technique, for instance, estimates the current from the drain-source voltage of a MOSFET switch and its accuracy therefore hinges on the on-resistance value of the MOSFET, which varies significantly with temperature, process, and supply voltage (e.g., 50% to 200%). In the case of the sense-FET technique, a mirror transistor is used to source a fraction of the switch current, and its accuracy relies on the matching performance of the current mirror, whose mirroring ratio is on the order of 1,000, and its operating region is in triode (i.e., ohmic/non-saturated). Although accuracies of ±4% are reported [17], the mismatch and process variations cause errors as large as ±20% (i.e., 3σ spreads), which result in large device size spread between the sense-FET and the power-FET in the mirror [19]. Moreover, the sense-FET technique is only practical if power switches are implemented on-chip, or if specially matched MOSFETs are available. Moreover, given the switching nature of these devices and their inherent switching noise (both in the MOSFET R_{on} and sense-FET techniques), their use in switching feedback control applications is limited.

The filter technique, which measures the inductor current by applying a low-pass filter across the inductor, is inherently less susceptible to switching noise and is therefore better suited for current-mode controllers with high switching frequencies [11, 18]. Nevertheless, its accuracy is dependent on the inductance and how well the filter is matched to the inductor. Even when the inductance is known and the filter is well matched, component tolerances and operating-point variations can cause up to ±28% error (±15% initial inductor tolerance, ±11% ESR variance, and a temperature range of

70°C) [18]. In practice, lower accuracies are expected to occur in wide temperature range applications (e.g., commercial range for power supply chips is from -10 to 125 °C).

Table 1.1— Summary of state-of-the-art lossless current-sensing techniques.

Method	Description	Disadvantages
MOSFET R_{on}	Senses the power MOSFET's drain-source voltage	- Low accuracy - Discontinuous and noisy
Sense-FET	Mirrors a fraction of the load current with a small sense MOSFET	- Low-accuracy - Only feasible for on-chip switches - Discontinuous and noisy
Filter	Filters the voltage across the inductor.	- Only for off-chip applications - Low accuracy (dependence on inductance)

The accuracy of lossless current-sensing techniques degrades if an integrated circuit (IC) current-sensing solution is required for use in a DC-DC controller application. Theoretically, lossless current-sensing circuits only sense voltages because sensing current implies additional series devices and therefore further power losses. Estimating the current flowing through an existing device from only voltages requires knowledge of the device impedance (i.e., series resistance, inductance, or capacitance). For a switching power supply, the inherent series path elements are the inductor, output capacitor, and power switches, which are normally off-chip and are selected by the end user, not the IC designer. Typically, the IC designer is not cognizant of these specific off-chip values during the IC design cycle. Consequently, for any lossless current-sensing technique to be accurate, the circuit should somehow measure one of the current-carrying elements in its path and sense the voltage across the same (i.e., Ohm's law: I = V/R), which is the driving force behind the proposed current-sensing technique.

1.2. Research Objective

The research objective is to implement a monolithic and lossless circuit to measure the power inductor current of DC-DC converters continuously, instantaneously, and accurately. The circuit implementation should apply to the switching regulators with both on-chip or off-chip power switches, and it should be insensitive to a wide range of inductor values.

To achieve lossless operation in the proposed technique, the power inductor, itself, is exploited as the current-sensing element (i.e., transducer), and thereby the need for a resistive sensing element is eliminated. A power inductor is modeled by an ideal inductance in series with a parasitic equivalent series resistor (ESR). Thus, the current flowing through the inductor is the low-passed filter version of the voltage across the inductor. If an equivalent filter is designed to match the inductor inductance and its ESR, and the same voltage is applied to its inputs, the replica filter's output will resemble the current through the inductor (Figure 1.1). However, since the value of the inductor and its ESR are unknown to the IC designer, tuning and calibration procedures are performed at the start-up of the converter to adjust the filter gain and bandwidth by measuring the inductor's inductance and ESR values, consequently, making the current-sensing technique accurate (Figure 1.2).

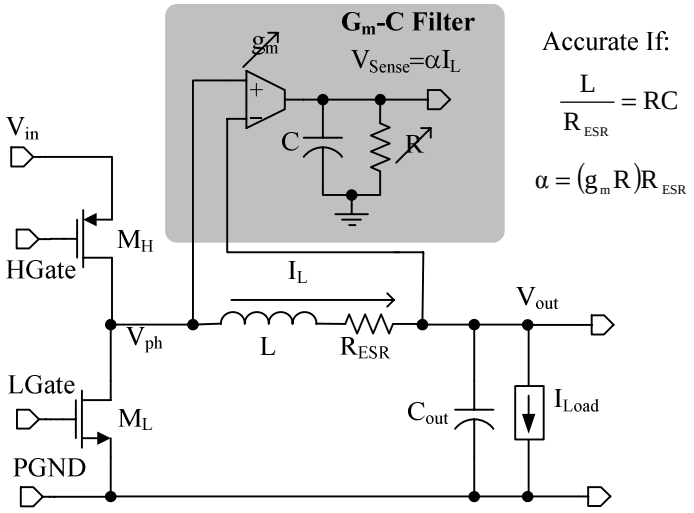


Figure 1.1—Application of a g_m-C filter to measure the inductor current in a buck switching converter.

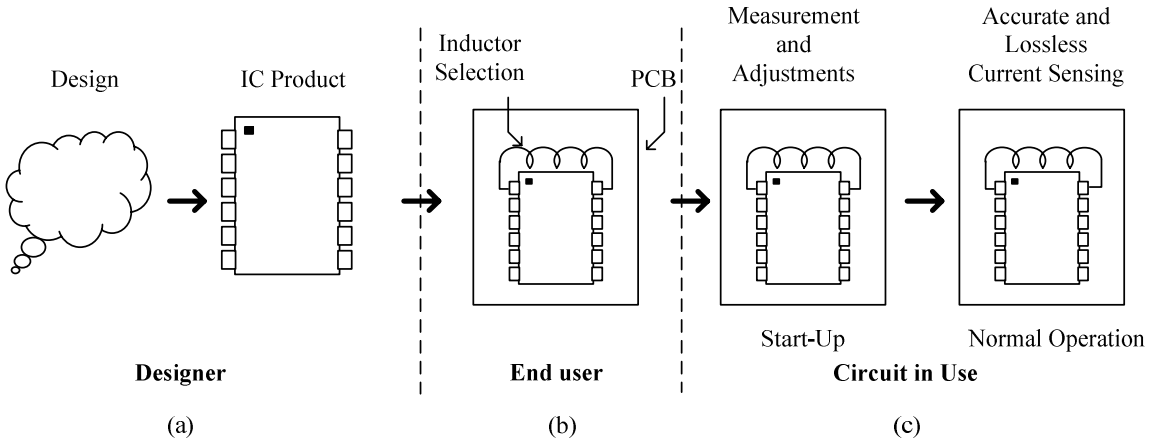


Figure 1.2—Proposed self-calibrating inductor current measurement: (a) IC designer is not aware of actual inductor value during design process, (b) end-user selects any off-chip inductor and placed it on PCB, and (c) IC measures the off-chip inductance and adjusts on-chip circuits accordingly.

The block diagram of the proposed IC is shown in Figure 1.3. The simplified block diagram of Figure 1.3(a) shows three distinct on-chip units: the current-sensing circuit, the current-mode controller, and the start-up control circuit. The power circuitry and the controller compensation network are implemented off-chip. The current-sensing circuit consists of the current-sensing filter, the tuning circuit, and the calibration block. The tuning and calibration sections are only active during system start-up, and therefore incur no power losses during regular operation. Once the proper tuning and calibration parameters are set, they are digitally stored, and the system is subsequently allowed to start and operate normally.

A current-mode pulse-width modulation (PWM) controller [8-9] is selected to test the functionality and reliability of the proposed current-sensing technique, since current-mode controllers are sensitive to current-sensing performance. Figure 1.3(b) illustrates the proposed chip in more detail. The start-up control circuit controls the start-up sequence of the proposed IC, as shown in Figure 1.3(c). After a power-on-reset event, both power switches (M_1 and M_2) are turned off, and transistor M_b is turned on (Figure 1.3(b)), which short circuits the output voltage (V_{out}) to ground. The M_1, M_2, and M_b states do not change until the end of the calibration phase. The start-up control circuit initiates the tuning cycle after the internal blocks of the chip have turned on (i.e., the

bandgap voltage is settled). The test-current generator forces an AC current into the power inductor during the tuning, and the frequency behavior of the current-sensing filter is subsequently tuned in a feedback loop until it matches the cut-off frequency of the power inductor. After the tuning is finished, the start-up circuit starts the calibration sequence by inserting a DC current into the inductor. The calibration controller trims the gain of the low-pass filter against a reference current. When tuning and calibration have both completed, the low-pass filter is ready to measure the inductor current at its output accurately. After calibration is finished, normal switching regulator operation begins. The transistor M_b is turned off at this point, and it remains off until the next time the system is reset.

The current-mode controller to be designed targets portable applications powered by a single Li-Ion battery such as cell phones and portable digital assistances (PDAs) and the proposed adjustable filter gain and bandwidth ranges are designed to cover inductors used for these applications. The targeted specification parameters of the proposed current-sensing circuit and current-mode controller are summarized in Tables 1.2 and 1.3.

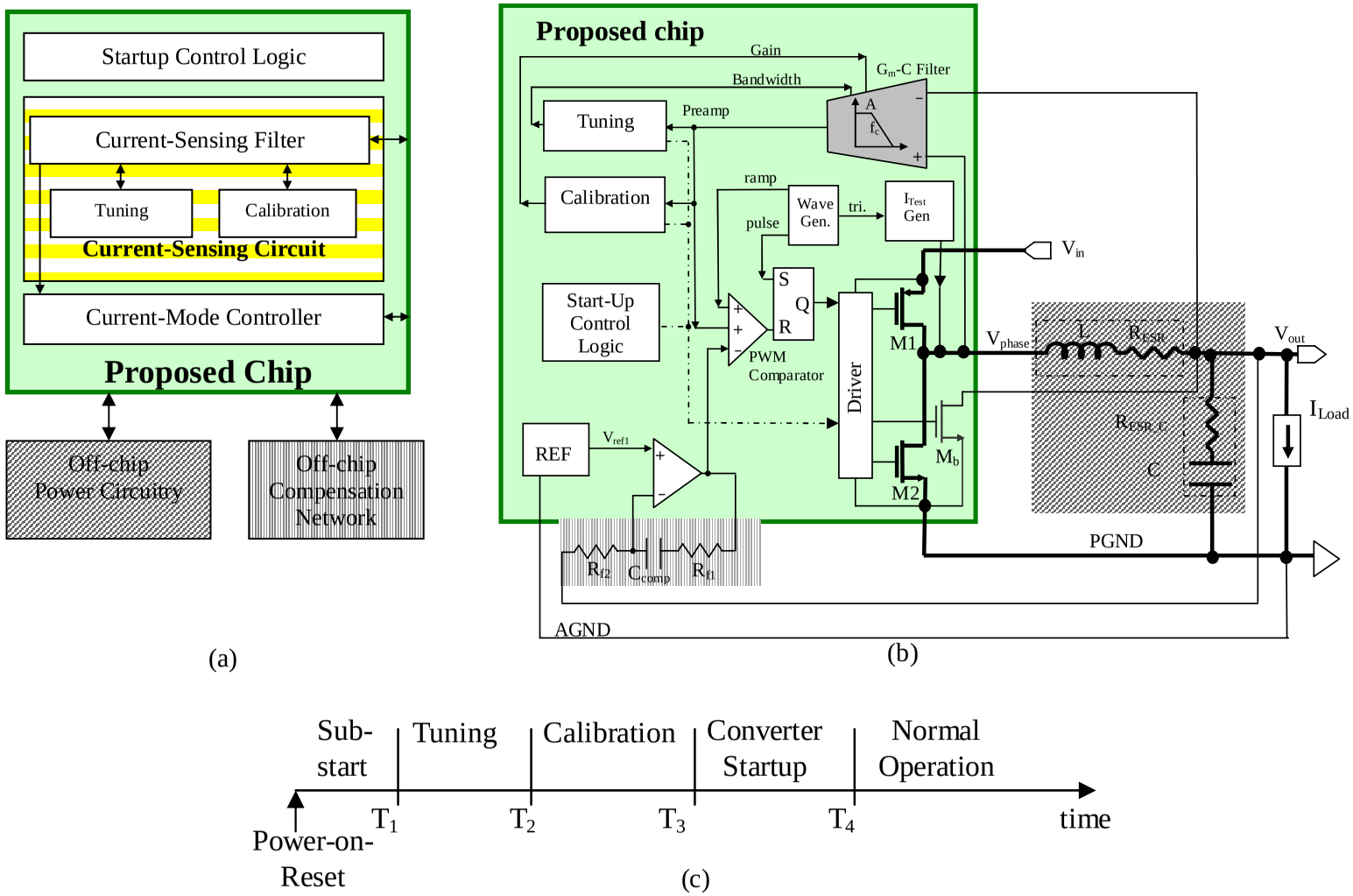


Figure 1.3— Block diagram of the proposed chip: (a) simplified, (b) detailed, and (c) start-up sequence.

Table 1.2—Proposed current-sensing module specifications.

Current-Sensing Circuit Specifications		
Spec. Comp.	**Target**	**Notes**
$R_{Sense} = V_{Sense}/I_L$	0.5 V/A	0.5 V for 1 A max current
Bandwidth for 1 MHz switching freq.	8 MHz	Less than 1% AC gain error Stability of current loop
R_{gain} Accuracy	±10%	
Start-up-Time	<1 s	System dependent
Supply (V_{DD})	2.7 V - 4.2 V	Li-Ion battery
I_L	0 A - 1.1 A	Cell-phone/ PDA/LED driver
L Range	2 μ H - 6 μ H	Mainstream type for portable applications
R_{ESR} Range	0.012 Ω - 0.188 Ω	Mainstream type for portable applications
ICMR of V_{Ph} Input	-1 - V_{DD}	Buck converter phase
ICMR of V_o Input	0 - V_{DD}	Buck converter output
Switch_EN	CMOS $V_{th} = V_{DD}/2$	
C_{in} of V_{Ph} Input	<10 pF	G_m-C filter input stage
C_{in} of V_o Input	<10 pF	G_m-C filter input stage
R_{in} of V_{Ph} Input	>20 kΩ	<100 μA current
R_{in} of V_o Input	>20 kΩ	<100 μA current

Table 1.3—Test switching regulator specifications.

Converter Type	Buck (step-down) converter
Input Voltage	2.7 V to 5 V (Li-Ion battery)
Output Voltage	1.5 V (0.25 μm technology)
Control Technique	PWM Current-mode control
Output Current	0 A to 1 A Cell-phone and PDA processor
Output Voltage Accuracy (DC + transient)	5% (±45 mV)
Efficiency	>80% at full load
Switching Frequency	1 MHz

1.3. Market Demand

No research is valuable in the field of engineering if it cannot be applied to real-life solutions and this section evaluates the demand for this research. Generally speaking, a great demand for voltage regulators exists in portable, battery-operated instruments such as laptops, cell phones, digital cameras, and PDAs, and the market is growing every year [20-25]. Switching regulators and power-management chips, which are mainly linear, accounted for approximately 9% of worldwide semiconductor revenue in 2004. Nearly 25% of the analog IC revenue in 2004 was derived from power-management

semiconductors, and discrete power devices accounted for the 75% of total discrete device revenue in the same year. For continued growth, solid-state electronics must perform better, yet be more affordable. On-chip integration generally reduces fabrication costs by eliminating discrete PCB components and replacing them with comparably free on-chip devices [26-29].

The proposed research addresses the market demand for high-performance switching regulators in several ways. Lossless current sensing increases the efficiency of switching regulators by 2% to 10% at high currents. Mode hopping, a procedure that increases efficiency at all load currents; inductor multiplication, a technique that enhances on-chip inductor performance; and robust compensation techniques can all be implemented, if current is measured accurately [30]. Additionally, the proposed technique is implemented totally on-chip, requiring no additional external components, which results in lower system cost. Moreover, automated current-sensing filter adjustments eliminates the time spent by end users to design and develop an accurate off-chip current-sensing circuit, which makes the approach more user-friendly. In a broader view, calibration and optimization procedures lead to self-learning management schemes that permit precise and lossless measurements and storage of off-chip component values, which are normally unknown to IC designers at the design cycle, during start-up, enabling power adaptive converter schemes and therefore optimum efficiency.

SUMMARY

Current-sensing circuits are essential for protection and control of switching regulators. Traditionally, a sensing resistor is inserted in the series path of the current to be measured. However, adding a sense resistor to a power circuit incurs significant power dissipation and reduces the converter's power efficiency. Nevertheless, currently available lossless current-sensing techniques are not accurate without the knowledge of off-chip components, which is generally not available to IC designers, since the end-user selects the inductor, capacitor, switches, and their respective specifications at the PCB level. To address this problem, this research aims to implement a monolithic and lossless circuit to measure the power inductor current of DC-DC converters continuously, instantaneously, and accurately. The proposed circuit measures the off-chip component

values during start-up and adjusts on-chip filters accordingly. State-of-the art current-sensing circuits and applications are discussed in more detail in the next chapter, followed by the introduction of the proposed self-calibrating, lossless, and accurate current-sensing technique.

CHAPTER 2

STATE-OF-THE-ART CURRENT-SENSING CIRCUITS

This chapter reviews the applications and state-of-the-art techniques for current-sensing in switching regulators. Sensing the inductor current is not only necessary for conventional applications such as protection and control but it is also critical that it be done in a lossless and accurate fashion when applied for advanced control techniques, which are devised to optimize transient response, increase efficiency over a wide range of load currents, eliminate the off-chip compensation network, and integrate the power inductor. However, as will be discussed in this chapter, the realization and large-scale application of all these techniques depend on a lossless and accurate current-sensing technique, which is not currently available and is therefore the objective of the present research.

2.1. Current-Sensing Applications in Switching Regulators

Besides protection and frequency compensation, which are traditionally the reasons for current-sensing in switching regulators, recent schemes devised to address demands for full integration of DC-DC converters and for achieving high efficiencies in portable applications depend heavily on knowledge of the inductor current. Moreover, while for some applications such as protection, a relatively inaccurate current sensing is sufficient, applications such as current-mode controllers require precise current sensing.

2.1.1. Protection

Every power supply includes an over-current detection circuit [31], which protects the system against over-current conditions. Digital signal processors (DSPs), which are the core of today's electronic systems such as cell phones, are relatively expensive circuitry, and power-management chips are designed to robustly protect their loads, even at the cost of permanently damaging themselves. The accuracy needs of over-current detection depend on the application. For instance, the current of backlight diodes should be accurately controlled because of its sensitivity to over-current drive. The

VRM9 standard, which defines the specification of Pentium processor power-management chips, requires that the switching converter shuts itself down itself when the inductor current exceeds 50% over the maximum specified load current.

2.1.2. Frequency Compensation

Basic DC-DC converter circuits are relatively simple and consist of a few power components [31, 32]. In practice, a feedback loop is applied around the power circuitry to regulate the output voltage and correct the duty cycle in events of load (output current) or line (supply voltage) disturbances. The sensed inductor current is a rich source of information for the operating state of the system and current-mode controllers [33-39] exploit this information. Many control methods are available and have been reported for DC-DC converter circuits. Some control techniques regulate output voltage using only output voltage information while more sophisticated control strategies require knowledge of inductor current. The control techniques reported in the literature are generally divided into pulse-width modulation (PWM), pulse-frequency modulation (PFM), and sliding-mode control. Each of these control techniques has its advantages and disadvantages. Among those techniques, operation of current-mode, constant on-time PFM, and sliding-mode controllers depend on the knowledge of the inductor current.

Table 2.1—Current sensing and control schemes for switching regulators.

Control Technique	I_L Required?
PWM Voltage Mode	No
PWM Current Mode	Yes
PFM Constant On-Time	Yes
Sliding-Mode Control – Hysteretic (Buck)	No
Sliding-Mode Control – Boost and Buck Boost	Yes

2.1.3. Droop Compensation

Droop regulation is a technique that deliberately adds a load-dependent slope to the output voltage versus using an output current regulation characteristic, so that additional dynamic headroom is available both at the low- and high-current regions, as shown in Figure 2.1 [33]. This slope can be achieved either by increasing the source

impedance or by means of electronic control of the regulation characteristic. The output DC voltage remains within the regulation limits over all values of load current, but is skewed to a higher value at light loads and to a lower value at heavy loads. When operating at light loads, an increasing current load transient will generate a negative-going voltage transition, and the output voltage will then be biased so that there is a maximum amount of headroom for this transient before reaching the lower regulation limit. Correspondingly, a reduction in current when operating at heavy loads will generate a positive-going transient, and there will then be increased headroom to accommodate it. Nevertheless, load current, which is the inductor DC current, should be sensed for reliable and accurate control of droop voltage.

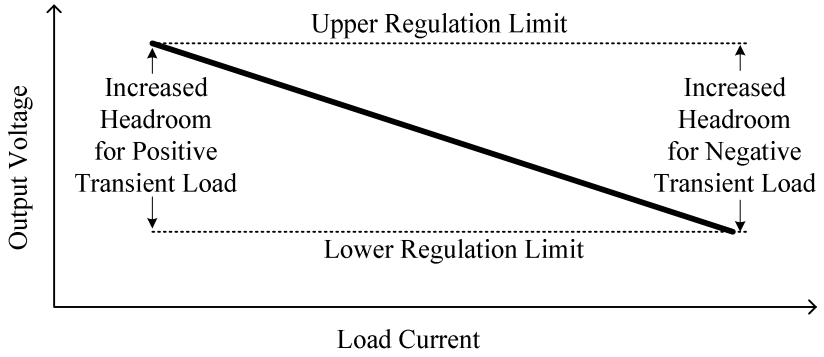


Figure 2.1—Dynamic headroom with droop compensation.

2.1.4. Mode Hop

Yet another useful application of current sensing in power supplies is demonstrated in mode-hopping techniques for high-performance DC-DC converters, where the operating region of the circuit adapts to the varying load current, which tunes the circuit optimally for enhanced power efficiencies [34]. At low load currents, switching losses are dominant and the frequency can then be reduced to increase the efficiency. At high-load currents, the conduction losses are dominant, and other control techniques may be appropriate. It is shown in [34] that for different control techniques of continuous- conduction mode (CCM), discontinuous-conduction mode (DCM), and

constant peak-current control, different efficiency maximum points exist. For low current loads, for instance, the constant peak control is best. However, the best efficiency is achieved for CCM with a certain frequency in higher load currents. The converter operation can also be changed from synchronous mode (two MOSFETs) for high load currents to asynchronous mode (a MOSFET and a diode) in low load currents to further increase the overall efficiency [34]. At high-load currents, conduction losses are dominant, and the synchronous mode has lower conduction loss in the low-side switch. However, switching losses are reduced in low-load currents where switching losses are dominant by only using one MOSFET switch and a diode in asynchronous mode.

2.1.5. Inductor Multipliers

An obstacle to full integration of DC-DC converters is the need for power inductors and capacitors that cannot be implemented economically on-chip. Recently [35], an inductor-multiplier technique was introduced that places active circuitry around the inductor to boost its value. Multiplying the inductance of a small inductor in a switching power supply circuit amounts to subtracting ripple current from the output terminal of the inductor, or in other words, adding a complement of the ripple current. The resulting ripple current of the multiplying circuit is smaller, which is characteristic of larger inductors. To generate the complement ripple current, first the inductor current should be sensed continuously precisely.

2.1.6. Single-Inductor Multiple-Output Converters

Power inductors are expensive and bulky elements. In an application that requires N output voltages, a straightforward implementation would be using N switching converters, thus requiring N inductors and 2N power devices (transistors and diodes). If the N outputs do not need to be individually controlled, then a transformer with one primary winding and N-1 secondary windings could be used. In such a case, one of the outputs (usually the one with the heaviest load) can be accurately controlled, while the rest would simply track the “master output”. Both implementations require bulky magnetic cores. For considerable savings in cost, weight, and size, recently a technique was proposed [36] for realizing single-inductor multiple-output converters without the

use of transformers. Nevertheless, all these techniques depend on precisely sensing the inductor current.

2.1.7. Current-Sharing Techniques

Distributed power architecture has numerous advantages in microprocessor-based systems [33]. High-performance desktop computers, workstations, and servers use multiple microprocessors to satisfy their computing throughput demands. These applications use one DC-DC converter for each microprocessor to take advantage of the modularity and economy of scale offered by a DC-DC converter. The converters' outputs are connected to common power and ground planes, which feed multiple processors. Tying all of the converter's outputs to common power planes requires a current-sharing mechanism to ensure that each regulator equally shares its portion of the load. These parallel DC-DC converters are configured so that they share, approximately equally, the total current demand of the processors. This sharing results in higher reliability because peak thermal demands are reduced. Moreover, all of the DC-DC converters can respond to dynamic load demands from any processor, resulting in enhanced transient response. The overall goal is to have all the DC-DC converters share current equally with less than 10% error [33], which is only achievable when an accurate current sensor is implemented on each regulator.

2.2. Current-Sensing Techniques for Switching Regulators

A basic block diagram of a step-down buck converter and its corresponding waveforms are illustrated in Figure 2.2 [31, 32]. The power circuit is simple and consists of high-side and low-side power switches (i.e., M_H and M_L), an inductor, and at least one capacitor. Because of the high values of the passive components (e.g., in μF and μH range), the power stage inductor and capacitor are almost always implemented off-chip. The controller supplies the power MOSFETs with gate signals to regulate the output voltage of the converter to a target reference voltage. Error amplifiers, comparators, voltage references, and drivers are among the building blocks of the controller and are usually implemented on-chip.

For most of the applications discussed in Section 2.1, the current to be measured

is the inductor current, I_L. However, for some of these applications, knowledge of inductor current is only required in a specific portion of a switching period, such as when the high-side switch, M_H, is turned on. Therefore, depending on the application, inductor current (I_L), high-side switch current (I_{MH}), low-side switch current (I_{ML}), output capacitor current (I_C), which is equal to inductor ripple current, or load current (I_{Load}) may be the current to be measured.

In practice, measuring inductor current through I_{MH} or I_{ML} is not trivial because of non-zero gate currents of switches at switching events. Since the drivers of power MOSFETs are designed to charge and discharge their high capacitance gates quickly, the transient gate current (I_G) is comparable to the inductor current. The gate terminal current eventually flows into the drain and source of the power MOSFETs and appears as switching spikes on their drain-source current, disturbing the inductor current measurement (Figure 2.3). The specifics of available current-sensing techniques are discussed next.

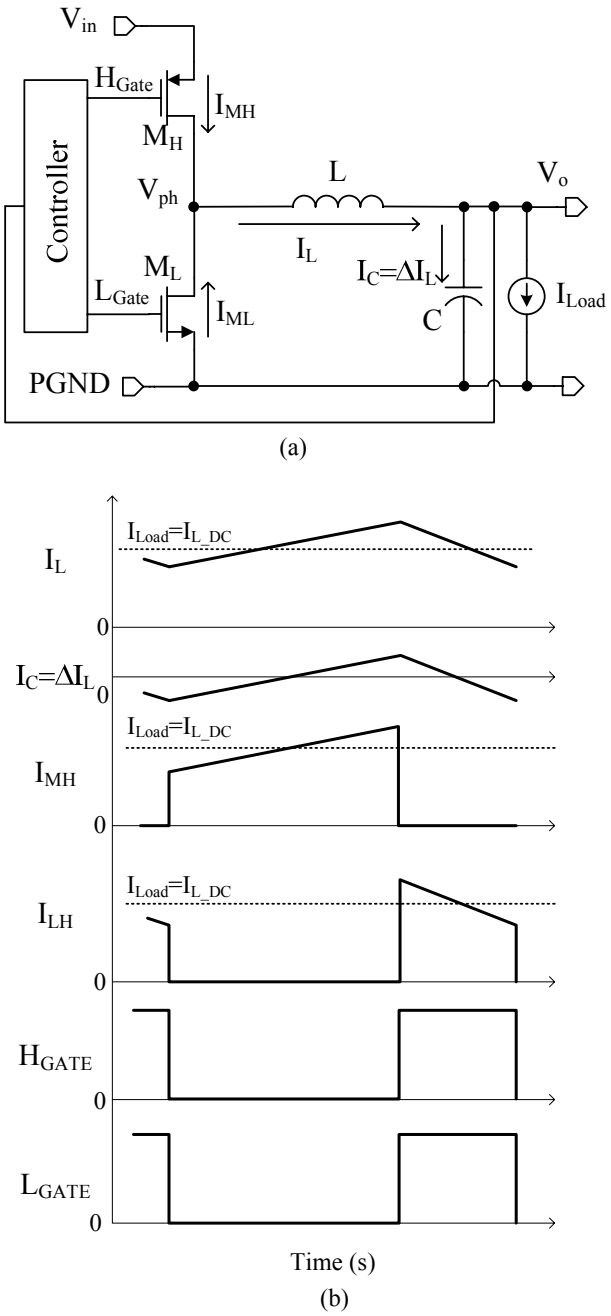


Figure 2.2—(a) Basic block diagram of a buck switching regulator and (b) corresponding timing waveforms.

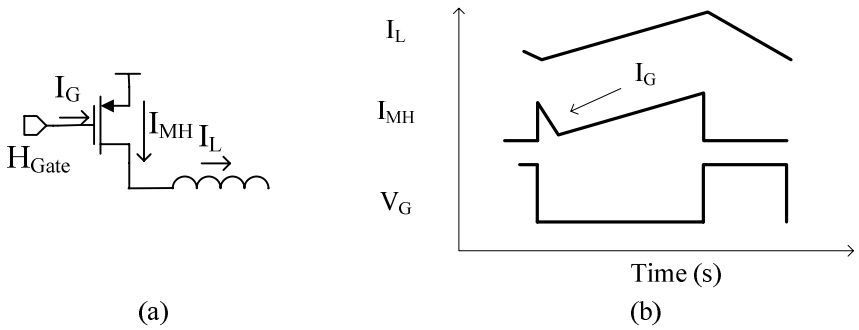


Figure 2.3—Sensing switch current instead of inductor current results in switching noise due to transient gate currents: (a) schematic and (b) waveforms.

2.2.1. Sense Resistors

The traditional way of current sensing introduces a resistor in the path of the current to be sensed (Figure 2.4). The sense resistor can be placed in series with the inductor, switches, and the load. Since current values in DC-DC converters are high (on the order of amperes), even a small resistor can cause severe power losses and reduce the efficiency by 2% to 10%. For a voltage of 100 mV across the sense resistor with 1 A inductor current, a sense resistor of 0.1 Ω is required, which results in 100 mW power dissipation in the sense resistor. The value of the sense resistor cannot be reduced to negligible values, since the accuracy of the detection reduces as the voltage drop across the resistor degrades, which is mainly caused by offset, noise, and high gain-bandwidth requirement.

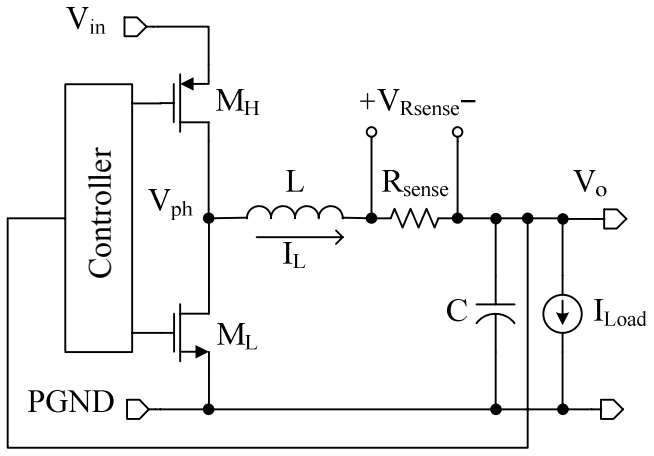


Figure 2.4—Traditional current-sensing technique: R_{sense}.

As integrated circuit fabrication technologies improve, transistor channel lengths are shortened to make digital circuits faster. However, reducing channel length results in lower breakdown voltage levels, requiring integrated circuits to be driven with lower supply voltages. Nevertheless, the current levels either remain the same or increase; therefore, the power loss in the sense resistor becomes more important as the voltage levels decrease, and current levels increase (Figure 2.5). Although the power loss in the sense resistor may seem small (e.g., 5%), it should be avoided to meet specifications for more than 90% efficiency required in many portable applications, especially portable applications. The power loss in switching converters is caused by conduction losses, which are proportional to parasitic resistances (i.e., current-sensing resistors, inductor equivalent series resistors (ESRs), etc.), as well as switching losses, which are proportional to frequency. The switching frequency is determined by the small component sizes required in small-area PCBs (e.g., cell phones and personal digital assistants (PDAs)) and by maximum allowable transient ripple. As a result, the switching frequency is determined almost without efficiency considerations, and designers rely on reducing the power losses mostly by decreasing conduction losses.

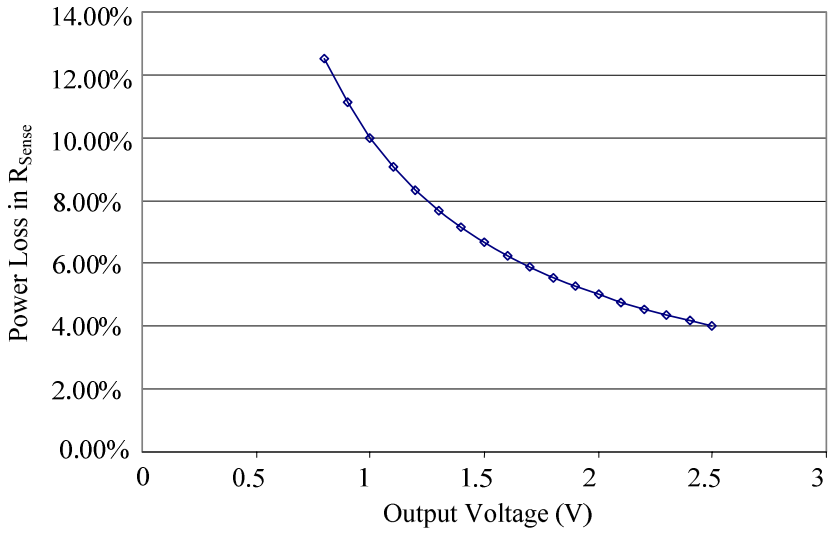


Figure 2.5—Percentage of output power loss in the sense resistor versus output voltage for 1 A output current and R_{sense} = 0.1 Ω.

Therefore, a lossless current-sensing technique can significantly help the designer meet challenging efficiency specifications. However, the current-sensing resistor is the most accurate available current-sensing technique, which is why it is used in current-sensitive applications.

2.2.2. MOSFET-RDS

MOSFETs act as resistors when they are "on" and are biased in the Ohmic (non-saturated) region. Assuming small drain-source voltages, as is the case of MOSFETs when used as switches, the equivalent resistance of the device is

$$R_{DS} = \frac{L}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)}, \tag{2.1}$$

where μ is the mobility; C_{ox} is the oxide capacitance per unit area; L and W are the MOSFET length and width; and V_T is the threshold voltage [31]. Consequently, the switch current is determined by sensing the voltage across the drain-source of the MOSFET, if R_{DS} of the MOSFET is known (Figure 2.6). The main drawbacks of this technique are low accuracy and switching noise from non-zero gate currents during transients. The R_{DS} of the MOSFET is inherently nonlinear. Furthermore, the R_{DS} of the MOSFET (on-chip or discrete) usually has significant variation because of μC_{ox} and V_T variations from die to die, not to mention how these values vary across temperature, which can yield a total variance of -50% to 100%. The R_{DS} depends on temperature exponentially (35% variation from 27°C to 100°C) [37]. The gate voltage of the MOSFET also changes because the input voltage of a converter changes over time, as the battery discharges (i.e., a Li-Ion battery voltage changes from 4.2 V at full charge to 2.7 V when it has lost all its stored energy). The effect of temperature and gate drive voltage on the resistance of a power MOSFET with an aspect ratio of 60,000 μm/0.6 μm built in AMI's 0.6 μm CMOS process is shown in Figure 2.7. In spite of low accuracy, this method enjoys commercial use for over-current protection because of its good power efficiency (no additional resistor is added, making it effectively lossless technique).

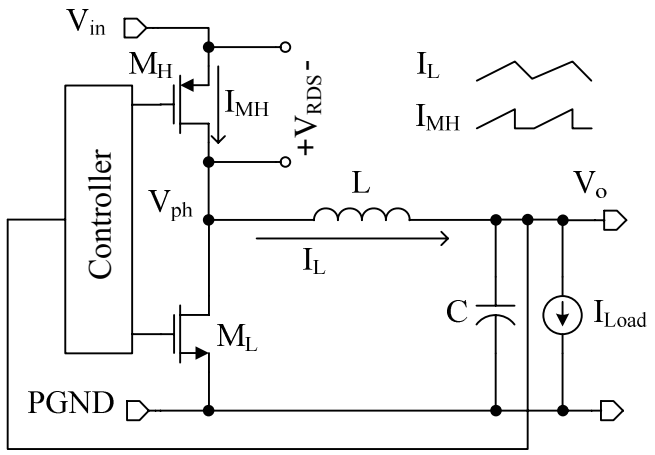


Figure 2.6—MOSFET RDS technique.

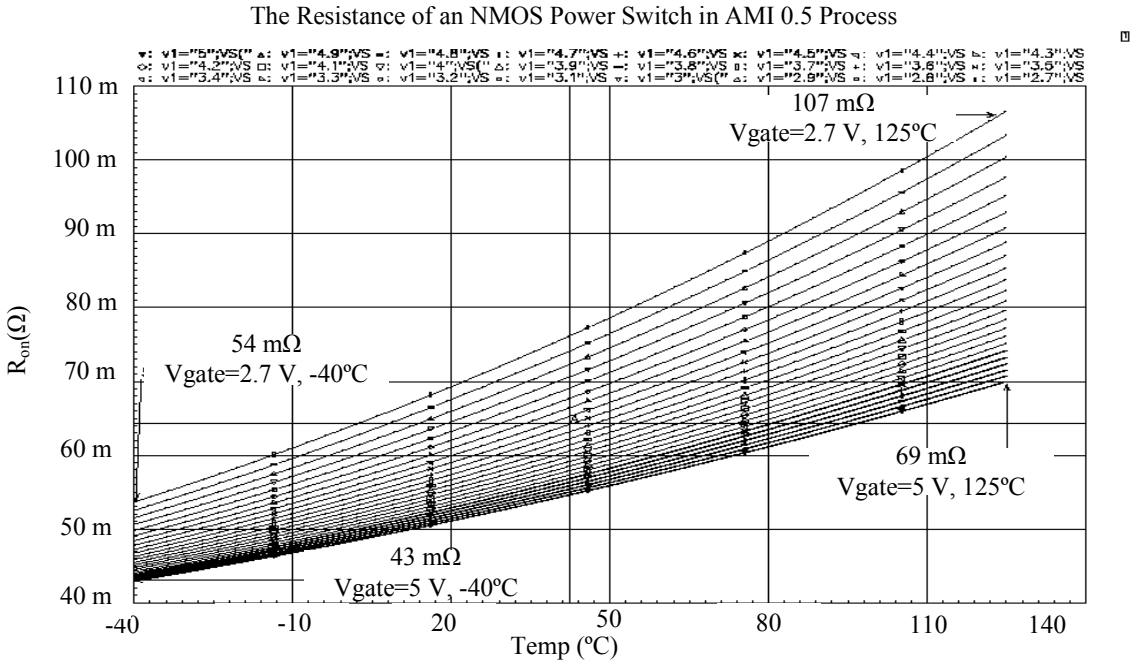


Figure 2.7—MOSFET "on" resistance across temperature and gate voltage for a power MOSFET built in AMI's 0.5- μm CMOS technology with a W/L of 60,000 μm/0.6 μm.

2.2.3. Sense-FET Technique

This method is a practical technique used for current sensing in many new power MOSFET applications [38-43]. The idea is to build a current-sensing FET in parallel with the power MOSFET (Figure 2.8). The effective width (W/N) of the sense MOSFET (sense-FET) is significantly smaller than the power FET (W). In practice, the width of power MOSFET is at least a thousand times larger than the width of the sense-FET (N>1000) to guarantee that the consumed power in the sense-FET circuit is low, i.e., quasi-lossless. The drain voltages of the main MOSFET and the sense MOSFET should be equal to eliminate gain errors in current mirror resulting from channel-length modulation. A more accurate current-sensing circuit using a sense-FET is shown in Figure 2.9, where M_H is the power MOSFET and M_{HS} is the sense-FET. In this circuit, an operational amplifier is used to force drain voltages of M_H and M_{HS} to be equal.

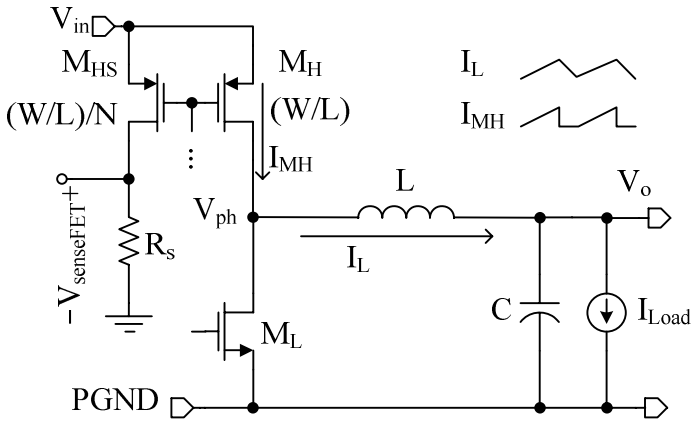


Figure 2.8—Sense-FET technique.

The high-frequency response of the current mirror should also be considered. As the width ratio of the main MOSFET to the sense-FET increases, the accuracy of the current-sensing circuit decreases since the matching accuracy between the main MOSFET and the sense-FET degrades. The accuracy of the sense-FET technique is about ±20% in practice, since a very large MOSFET is matched to a very small sense-FET. Moreover, the sense-FET technique introduces a large amount of switching noise at its output because of the non-zero gate current of the main MOSFET during switching

events. For converters with high load currents where the switches are off-chip, the implementation of the technique may not be possible because of unavailability of discrete sense-FET switches.

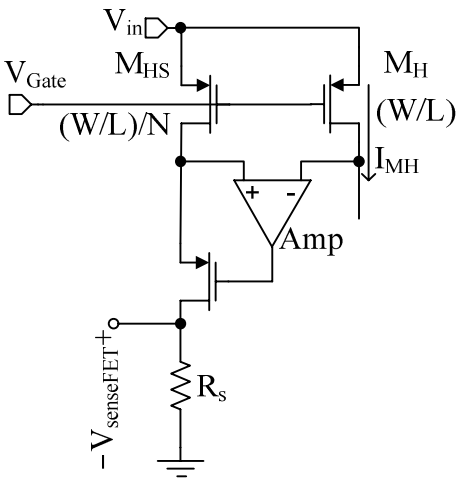


Figure 2.9—A circuit designed to improve the accuracy of a sense-FET.

2.2.4. Hall-Effect Sensors

Hall-effect sensors are among the popular solutions for current measurements. The oscilloscope DC current probes usually use Hall-effect sensors. A current in a conductor produces a magnetic field around it. When a second current-carrying conductor is placed into the magnetic field, the electrons are pushed to one side of the second conductor more than the other side, which generates a voltage across its width. This voltage across is proportional to the magnetic field value, which is proportional to the current flowing into the first converter. This phenomenon is known as the Hall effect, for its discoverer. Discrete Hall-effect sensors use ferromagnetic condensers to increase sensitivity. There are some Hall-effect sensors reported in CMOS [44-48]. Generally, the sensitivity of the Hall-effect sensor in CMOS is very low even with additional micromachining steps to add ferromagnetic material for condensers. Moreover, CMOS Hall-effect sensors suffer from temperature-dependent offset and low bandwidths (10 kHz to 50 kHz) caused by additional offset-cancellation circuitry. To the best of the author's knowledge, adoption of integrated CMOS Hall-effect sensors for current-sensing

in DC-DC converters has not been reported, mainly because of their low sensitivity, low bandwidth, and low accuracy resulting from temperature offset variations (i.e., drift).

2.2.5. Transformer Technique

Current transformers (CT), which are implemented differently from voltage transformers and are commonly used in high-power systems to measure current, can be used to sense the inductor current of a switching regulator in a lossless manner (Figure 2.10). The major drawbacks are increased cost and size and the inability to integrate the transformer. Additionally, the transformer cannot detect the DC value of the current, which makes this method inadequate for over-current protection.

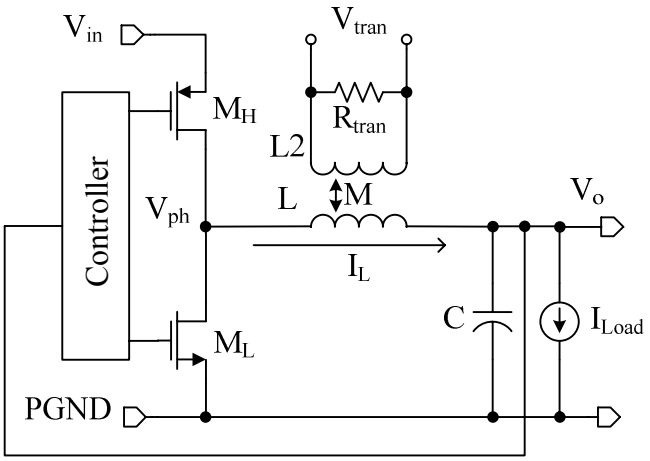


Figure 2.10—Measuring the inductor current with a transformer.

2.2.6. Observer Approach

This method, which was introduced by Midya [49], estimates the inductor current by integrating the voltage across it (i.e., v = Ldi/dt). However, to avoid saturation in the integrator because of inductor equivalent series resistor DC voltage, the integrator is reset periodically, and therefore only AC ripple current is estimated. Nevertheless, the inductor value must be known for an accurate ripple current measurement.

2.2.7. I-Average Technique

This current-sensing technique, illustrated in Figure 2.11, uses an RC low-pass filter at the junction of the converter switches (V_{ph}). Therefore, the voltage at filter output capacitor (V_{CA}) is the average voltage of the phase node. Consequently, the differential voltage at the input of the amplifier is the DC voltage across the inductor. In other words, the output sense voltage is

$$V_{I\text{-}Average} = K(R_{ESR}I_{L\_DC}), \tag{2.2}$$

where R_{ESR} is the inductor ESR; K is the amplifier gain; and I_{L_DC} is the DC inductor current. This scheme is often used in multi-phase DC-DC converters to share the load current [43].

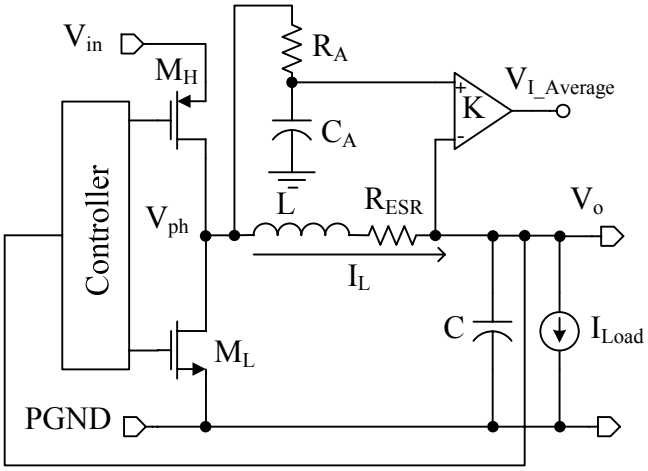


Figure 2.11—Averaging the inductor voltage to sense the current.

2.2.8. Matching Complimentary Filter

This technique was reported in *Fairchild Application Notes* and also analyzed extensively by E. Dallago [37, 50]. Using a simple low-pass RC network to filter the voltage across the inductor, the technique senses the current through the inductor and its ESR (Figure 2.12). An amplifier is used to amplify the voltage across the filter capacitor

if necessary.

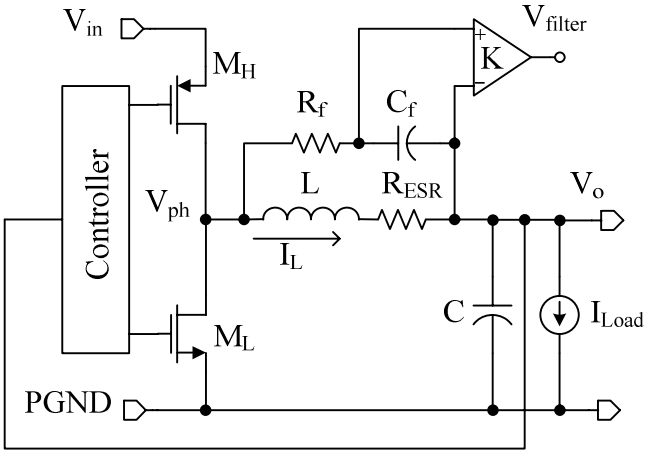


Figure 2.12— Complementarily filtering the inductor voltage to sense its current.

The voltage across the inductor is

$$V_L = (R_{ESR}+sL)I_L\,, \tag{2.3}$$

where L is the inductor value; R_{ESR} is the ESR of the inductor; and I_L is the inductor current. The voltage across the capacitor C_f is

$$V_{C_f} = \frac{V_L}{1+R_fC_fs} = \left(\frac{R_{ESR}+Ls}{1+R_fC_fs}\right)I_L$$

$$= R_{ESR}\left(\frac{1+(L/R_{ESR})s}{1+R_fC_fs}\right)I_L = R_{ESR}\left(\frac{1+T_Ls}{1+T_Fs}\right)I_L\,, \tag{2.4}$$

where T_L is L/R_{ESR} and T_F is R_fC_f. Forcing $T_L = T_F$ yields $V_{C_f} = R_{ESR}I_L$, and hence the capacitor output is directly proportional to the inductor current (I_L). To use this technique, the value of L and R_{ESR} need to be known, and R_f and C_f are then chosen accordingly. This technique, in its basic form, is not appropriate for integrated circuits because of the tolerance (i.e., variations) of the components. It is, however, a viable design for a custom discrete solution where the type and value of the inductor is known beforehand.

2.3. Problems of State-of-the-Art Techniques and Motivations for This Research

Different levels of accuracy and precision are required for current sensing circuits in various applications. A distinction here is made between accuracy and precision. Accuracy refers to how closely a measured value agrees with the correct value while precision refers to how closely individual measurements agree with each other. If the current-sensing information is used for the frequency compensation of switching regulators, such as in current-mode controllers, it should be precise, since small changes in inductor current are used for controller decision-making. Therefore, the sensed current should have low sensitivity to switching transients, since noise at the current-sensing output disturbs the controller operation (i.e., the output of the current-sensing circuit is directly connected to the PWM comparator). The same level of precision is required for single-inductor multiple-output regulators. Nevertheless, high accuracy is not needed in the aforementioned applications. In inductor multipliers, current-sensing should be both accurate and precise because the sensed current is used to generate a current that closely compensates the inductor ripple. The relative accuracy of current-sensing is especially important in multi-phase current-sharing DC-DC converters. If the currents are not balanced because of current-measurement errors, the load current is not equally distributed among the individual phases, and some of the phases will experience overloads, which reduce system lifetime and reliability.

On the other hand, if current-sensing information is used for over-current protection, a relatively accurate and moderately precise current-sensing is sufficient. An exception to this relaxed requirement is when design specifications require maximum usage of the safe-operation area (SOA) of the power components or of the load to reduce cost. Similarly, inaccurate current-sensing reduces the performance of mode-hopping schemes by interchanging the control schemes at non-optimum points without losing functionality although it does not cause system malfunction. The current-sensing accuracy and precision requirements of various applications are summarized in Table 2.2.

Table 2.2—Comparison of the properties of state-of-the-art current-sensing techniques.

Application	Requires Precision I_L?	Requires Accurate I_L?
Protection	No	Application Dependent
Frequency Compensation	Yes	No
Droop Compensation	Yes	No
Mode Hopping	No	Yes
Inductor Multipliers	Yes	Yes
Single-Inductor Multiple-Output Schemes	Yes	No
Multi-phase Current-Sharing Converters	Yes	No

High-performance switching regulators may exploit the current information for all of the aforementioned applications; therefore, a lossless, accurate, fast, and noiseless current-sensing technique is attractive for state-of-the-art switching regulators. Moreover, to reduce overall cost of the regulator, the current-sensing circuit should be realized on-chip. Available techniques, in their basic form, do not enjoy all of the above characteristics; the lossless schemes are not accurate and accurate techniques are not lossless (Table 2.3). Among the available lossless techniques, the filter technique embodies most of the desirable characteristics (i.e., it is instantaneous, continuous, noiseless, and provides both DC and AC current information). However, because of its dependency on inductance and ESR, the filter technique, in its basic form, is not suitable for integrated solutions since the integrated circuit designer is not cognizant of these off-chip components during the design phase and the inductor is selected by the end-user. The solution proposed in this dissertation is to integrate the filter on-chip and devise calibration circuits that measure the inductor and complimentarily match an on-chip filter to the off-chip inductor. The concept of self-calibrating is discussed in more detail in the next chapter.

Table 2.3—Comparison between state-of-the-art current-sensing techniques.

Technique / Properties	R_{SENSE}	R_{DS}	Trans former	Sense-FET	Hall Effect	L_{Filter}	$I_{Average}$
Monolithic	Yes	Yes	No	Yes	No	No	No
Lossless	No	Yes	Yes	Yes	Yes	Yes	Yes
Accuracy	Yes	No	No	No	No	No	No
Low Noise	Depends[1]	No	Yes	No	Yes	Yes	Yes
Measures DC/Ripple Current	Both	Both	Ripple Only	Both	Both	Both	DC Only
Continuous	No	No	Yes	No	Yes	Yes	Yes
Instantaneous	Yes	Yes	Yes	Yes	Yes	Yes	No

(1) Placing the sense resistor in the inductor path creates low noise current-sensing. However, if it is placed in the paths of the power switches, the switching noise appears at the output because the sense resistor conducts the gate current of the switches during transient events.

SUMMARY

This chapter established the need for an integrable, lossless, and accurate current-sensing scheme and discussed state-of-the-art techniques. Theoretically, lossless current-sensing circuits must only sense voltages because sensing current implies additional series devices, and therefore, further power losses. Estimating the current flowing through an already existing device from voltages only requires knowledge of the device impedance (i.e., series resistance, inductance, and capacitance), which are off-chip components not known to IC designer. Consequently, for any lossless current-sensing technique to be accurate, the circuit should (1) measure one of the current-carrying elements in its path and (2) sense the voltage across the same (i.e., Ohm's law: $I = V/R$). This two-step process is the driving force behind the proposed current-sensing technique and is conceptually described in next chapter.

CHAPTER 3

SELF-CALIBRATING, LOSSLESS, AND ACCURATE CURRENT-SENSING CIRCUIT

As discussed in the previous chapter, lossless current-sensing techniques are not accurate without the knowledge of inductor, capacitor, or switch values. Furthermore, techniques such as MOSFET R_{DS} and Sense-FET are inherently noisy because of transient gate currents, which limit their precision [51]. The filter technique [52], which measures inductor current by applying a low pass filter across the inductor, is intrinsically less susceptible to switching noise and is therefore better suited for current-mode controllers with high switching frequencies. Nevertheless, its accuracy is dependent on the inductance, and matching a filter to it is critical. Because of process-related tolerances, errors as high as ±28% are reported, even when the nominal inductor value is known, which is not the case for the IC designer, whose errors may then grossly exceed this value. The foregoing research proposes a technique to boost the accuracy of these current-sensing filters and to make them suitable for integrated circuits by automatically adjusting their bandwidth and gain via phase and gain feedback control loops. The proposed self-calibrating scheme essentially measures the inductance and ESR values during start-up and power-on-reset events. Because the filter is automatically tuned to the inductor, the current during normal operation can be measured accurately by simply sensing the voltage across the inductor. In this chapter, two methods, called high frequency tuning and low frequency tuning are proposed to adjust the current-sensing filter to the inductor parameters. To verify and investigate the proposed technique, a PCB prototype for low frequency tuning was implemented and its results are provided. The realization of the integrated version of the proposed technique through high frequency tuning is deferred to Chapter 6.

3.1. Proposed Approach

The proposed technique overcomes the accuracy limitations of lossless techniques

by automatically measuring the off-chip component values during start-up (Figure 3.1). The acquired information is then used to adjust the sensing circuit to estimate the current accurately during regular operation. The filter technique is chosen for integration and accuracy enhancement because of its high power efficiency, low susceptibility to switching noise, and compatibility with high frequency switching applications.

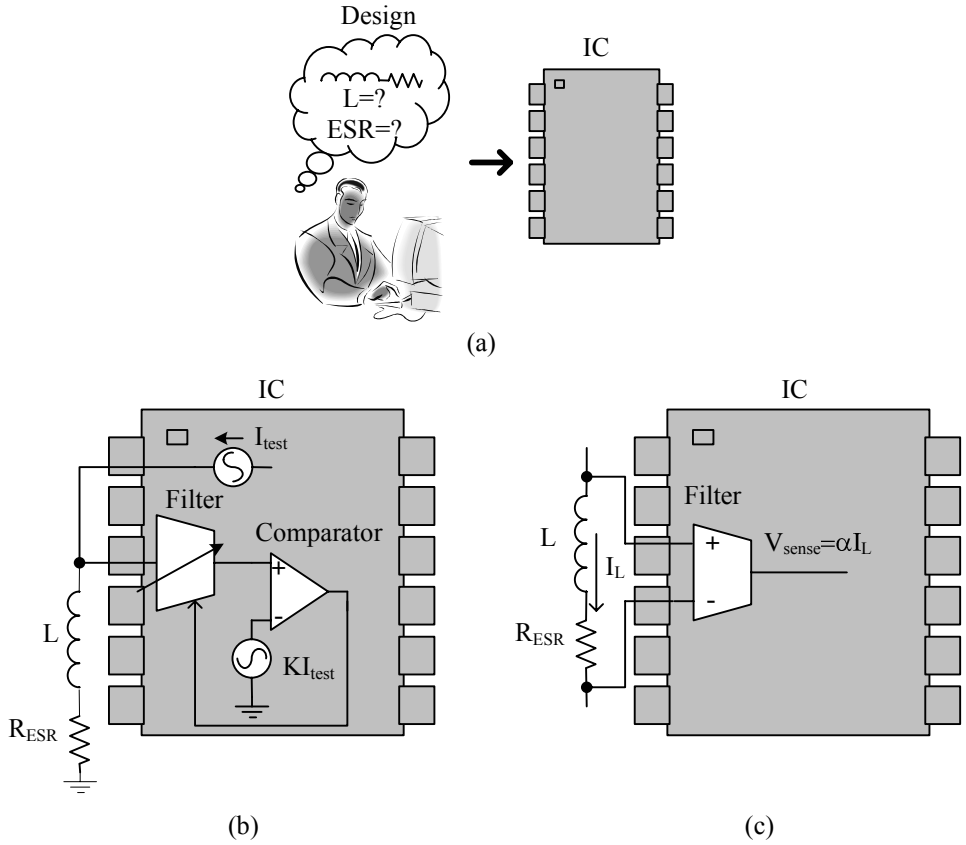


Figure 3.1—Self-calibrating current sensing: (a) designer, unaware of inductance value, implements calibration circuits; (b) calibration circuits adjust an on-chip filter to the off-chip inductor's cut-off frequency once the part is powered up; and (c) inductor current is measured accurately with calibrated filter during normal operating conditions.

The block diagram of the proposed current-sensing filter implemented with a g_m-C filter structure is shown in Figure 3.2. If an equivalent filter is designed to match the

series impedance of the inductor and its equivalent series resistor (ESR) and the same voltage is applied to its inputs, the output of the replica filter mimics the current flowing through the inductor. From Figure 3.2, output sense voltage (V_{Sense}) and inductor current (I_L) are low-pass filter versions of inductor voltage:

$$V_{Sense} = g_m R\left(\frac{1}{1+sRC}\right)V_L \tag{3.1}$$

and

$$I_L = \left(\frac{1}{R_{ESR}+sL}\right)V_L, \tag{3.2}$$

where V_L is the voltage across inductor; L is the inductance; R_{ESR} is the inductor's ESR; C is the filter capacitor; R is the filter resistor; and g_m is the filter's transconductance. If R is tuned to ensure L/R_{ESR} equals RC, the current-sensing filter output is directly proportional to inductor current I_L,

$$V_{Sense} = (g_m R)R_{ESR} I_L. \tag{3.3}$$

Additionally, if $(g_m R)R_{ESR}$ is $\alpha\ \Omega$, the estimated current is

$$V_{Sense} = \alpha I_L. \tag{3.4}$$

In Equation 3.1, varying R changes the cutoff frequency while adjusting g_m modulates the filter gain, which are the automatic adjustments proposed and presented in this chapter.

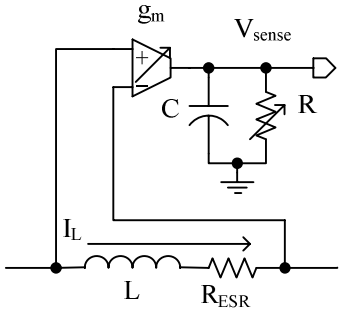


Figure 3.2—Block diagram of proposed current-sensing circuit.

3.1.1. Start-Up

Figure 3.3 shows how the proposed scheme is applied to a buck DC-DC converter. To measure the inductor and its ESR, a test current is forced into the inductor during start-up. At this time, power switches M_H and M_L are both off and switches M_a and M_b are on. Therefore, test current I_{test} flows entirely into the inductor, which makes the measurement of inductor characteristics possible by measuring the voltage across it. Since the test current is just a fraction of the maximum rated load (in this case, $I_{Load\text{-}max}/20$), M_a and M_b need not be as large as M_H and M_L. During normal operation, switches M_a and M_b are turned off and the current-sensing filter resumes its normal operation.

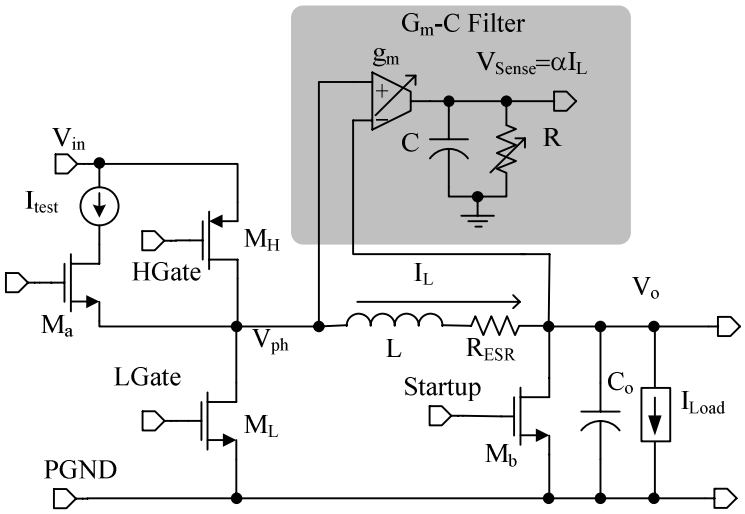


Figure 3.3—Applying the proposed technique to a buck DC-DC converter.

Figure 3.4 illustrates the system-level process of tuning and calibration. In mathematical terms, the current-sensing filter should be the inverse function of the inductor's trans-impedance (Figure 3.4). Therefore, a self-calibrating circuit should make the current-sensing filter transfer function equal to the inverse function of the inductor's impedance. There are two parameters, L and R_{ESR}, that should be measured, and two parameters, filter gain and bandwidth, that should be adjusted. Consequently, two stages are necessary for the adjustment process, which are called tuning and calibration in this

thesis.

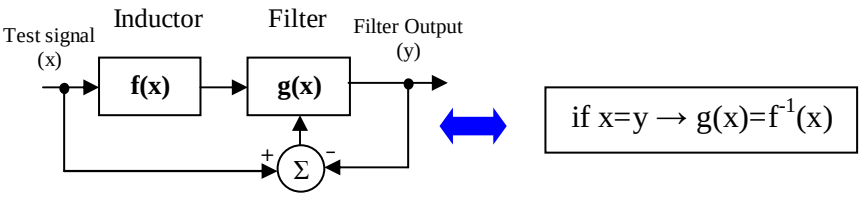


Figure 3.4—Mathematical illustration of the system configuration during tuning and calibration.

The Bode plot of the inductor impedance and the filter transfer function are shown in Figure 3.5. The inductor impedance is a non-ideal differentiator, while the filter transfer function is a non-ideal integrator. The cut-off frequencies of the available power inductors are in the range of 1 kHz to 10 kHz, while the operating frequency of a switching regulator is usually from 100 kHz to 1 MHz.

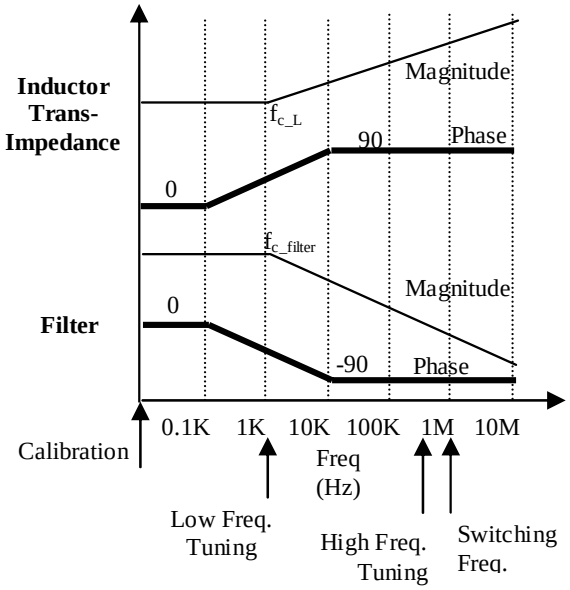


Figure 3.5—Bode plot of the inductor impedance and filter transfer function.

The tuning and calibration procedures can be performed in two ways: using low frequency or high frequency test signals to adjust the filter based on phase and gain detection, respectively. While the tuning is different, the calibration phase remains almost the same in both methods. The frequency behavior of the current-sensing circuit during tuning and calibration is shown in Figure 3.6 for both the low frequency (Figure 3.6(a)) and high frequency (Figure 3.6(b)) tuning schemes. In low frequency tuning, first the filter bandwidth is adjusted to the proper value, and then while keeping the bandwidth constant, the filter gain is calibrated. On the other hand, in high frequency tuning, the filter gain bandwidth is adjusted, and then while keeping gain bandwidth constant, the filter gain is calibrated until proper gain and bandwidth are reached.

In low frequency tuning, which is based on phase difference of the input and output signals, an AC test current with frequency close to the inductor cut-off frequency is inserted into the inductor. Figure 3.5 shows that there is a phase difference between the input test signal and the current-sensing filter output signal if the filter cut-off frequency is not matched to the inductor cut-off frequency. For highest phase detection resolution, sinusoidal test signals should be used since other periodical signals with the same frequency contain higher frequency harmonics that are less sensitive to inductor-filter mismatch. In the low frequency tuning scheme, first the filter cut-off frequency is matched to the inductor cut-off frequency, and then during the calibration, the DC gain of the current-sensing filter is adjusted to the inverse of the inductor ESR value. The control loops of low frequency tuning and calibration are shown in Figure 3.7. Since the input signal at the inductor is in the form of current and the filter output is in the form of voltage, the reference resistor (R_{ref}) is introduced as the voltage-to-current converter block. This resistor is physically present in the test-current generator block (I_{Test}) of Figure 3.3. The block indicated with K is a fixed-gain stage that compensates the attenuation caused by the reference resistor. In low frequency tuning, the input and output signal phases are compared, and the control loop varies the current-sensing filter bandwidth until the phases of input and output signals are equal. In calibration, DC test signals are used, and the filter gain is adjusted until the current-sensing filter output and the input test signals are equal.

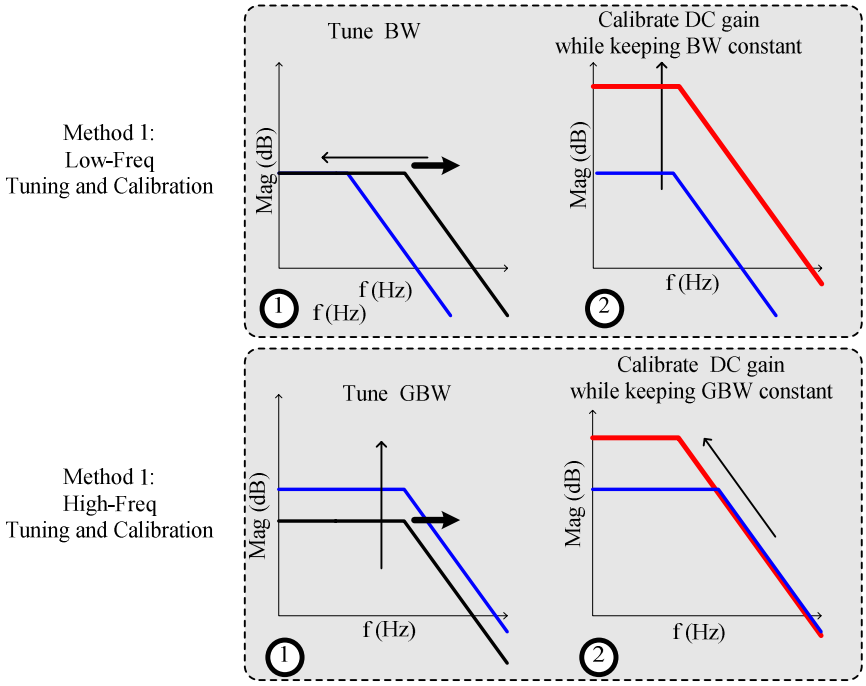


Figure 3.6—Illustration of current-sensing filter frequency response during tuning and calibration.

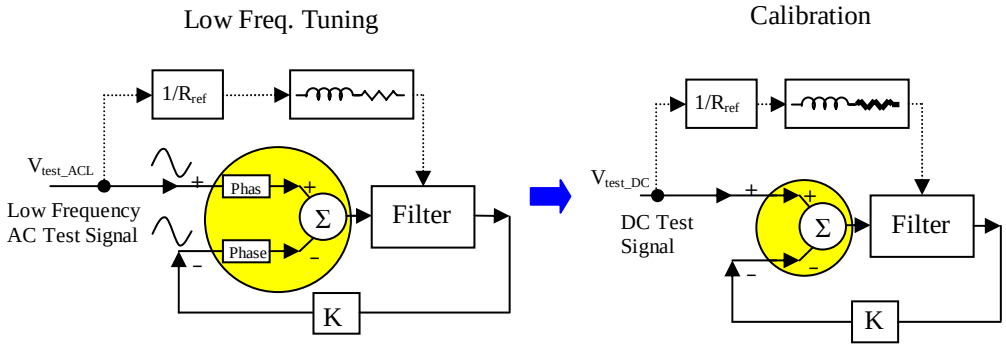


Figure 3.7—Dynamics of low frequency tuning and calibration.

In high frequency tuning, an AC test current with a frequency close to the operating frequency of the converter is used. In this case, there is no phase difference between the input and output signals when the current-sensing filter is not matched, since the test signal is at least a decade higher than the inductor cut-off frequency (i.e., the phase shift is 90° in inductor trans-impedance and -90° in current-sensing filter), and therefore signal amplitudes are processed. During the high frequency tuning scheme, the

filter unity-gain frequency is matched to the inductor trans-impedance frequency first, and then during the calibration, the DC gain of the current-sensing filter is adjusted to be the inverse of inductor ESR value. The control loops of high-frequency tuning and calibration are shown in Figure 3.8. Since the loops detect a mismatch from amplitude difference of input and output signal instead of the phase difference, triangular signals can be used instead of sinusoidal inputs during tuning.

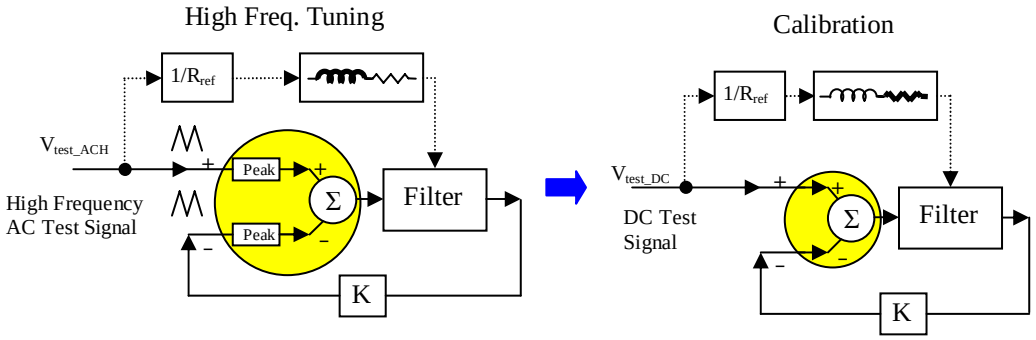


Figure 3.8—Dynamics of high frequency tuning and calibration.

Either the low or high frequency tuning and calibration schemes can be selected in start-up to enhance the current-sensing accuracy. Low frequency tuning was used in the *PCB prototype* implementation using discrete components. However, high frequency tuning seems more practical for integrated implementation because the cut-off frequency high-pass filter required in its tuning scheme is higher compared to the low frequency method and therefore is more suitable for integrated solutions (i.e., 50 kHz instead of 50 Hz). Moreover, the AC test signal in high-frequency tuning method is a triangular signal, which can be implemented on-chip more conveniently than a sinusoidal signal. Consequently, the high-frequency tuning and calibration scheme was used for *integrated-circuit (IC) prototype.* The implementation of PCB prototype is discussed in the next subsection and realization of the IC prototype is deferred to Chapter 6.

3.2. Discrete Verification

A prototype implementation of the system was designed using discrete

components and experiments verified the effectiveness of the proposed concept. This realization included tuning, calibration, and normal operation circuits, but the logic for transferring between these modes and test signals used were not implemented in the PCB prototype because the goal was to quickly verify the concept and evaluate its feasibility. Furthermore, filter adjustments are based on the low frequency tuning scheme.

3.2.1. Current-Sensing Filter

In the PCB prototype, the current-sensing filter was implemented with a g_m-C circuit (Figure 3.9). Transconductance cell g_{m2} is used in a shunt feedback configuration to realize the variable loading resistor R (Figure 3.2) and buffer Op1 isolates the loading effects of the g_{m2}-R circuit (Figure 3.9) on g_{m1}. Intersil® CA3280 g_m cells were used since their transconductances are externally adjustable via their bias currents. The differential pair-based g_m cells have good linearity but only for a limited differential voltage range (±50 mV), which is why a resistor divider network with a ratio of 1/820 was used to increase the range for which the cells are linear (0.15% linear over a ±3.3 V range). The linearity of the g_m-cell is important to prevent systematic offsets, discussed in more detail in Chapter 4. The resistor divider, unfortunately, increases the effective input-referred offset of the g_m cells by a factor equal to the divider ratio (i.e., by 820 in this case). Other feedback linearization schemes can be employed when designing the circuits at die level (IC), but their feasibility in a discrete-level design is limited.

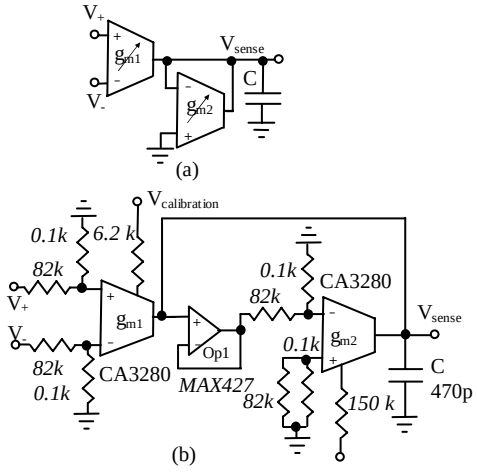


Figure 3.9—Design of gm-C filters: (a) basic concept and (b) circuit implementation.

3.2.2. Start-Up Hardware Implementation

Tuning the Circuit

In the tuning phase, the cut-off frequency of the low-pass filter is adjusted via a phase-mixed feedback control loop, until it matches the cut-off frequency of the power inductor (i.e., $f_c = R_L/L$). A sinusoidal voltage signal at frequency f_{ref} forces a sinusoidal current into the inductor, since reference resistor R_{ref} (100 Ω) is much greater than the inductor's equivalent series resistor, R_L, which is approximately 45 mΩ. The current through R_{ref} is therefore linearly proportional to the voltage signal (Figure 3.10). The tuning operation is not sensitive to signal frequency, f_{ref}, and it can range from 100 Hz to 1 kHz because the circuit will simply use the input reference current as a reference phase signal. A low-offset amplifier (MAX427- offset voltage is less than 15 μV) is then used to amplify the voltage across the inductor. This amplified voltage (V_3) has a phase lead of $\tan^{-1}(2\pi f_{ref}L/R_L)$ with respect to the reference sinusoidal signal because of the inductor's response. The g_m-C filter then introduces a phase lag of $\tan^{-1}(2\pi f_{ref}C/g_{m2})$, producing a total phase shift of

$$\text{Phase}(V_{sense}) = \tan^{-1}\left(\frac{2\pi f_{ref} L}{R_L}\right) - \tan^{-1}\left(\frac{2\pi f_{ref} C}{g_{m2}}\right). \qquad (3.5)$$

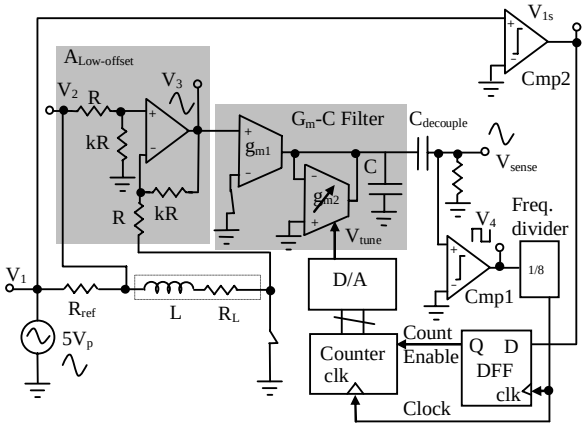


Figure 3.10—PCB prototype tuning circuit.

The phase detection process is performed by converting the sinusoidal input and output signals to square waves (V_{1s} and V_4) and synchronizing their rising edges. A frequency divider slows down V_4 and generates the *clock* signal for the circuit. V_{1s} is then sampled at the rising edge of the clock signal via a flip-flop. The output of the flip-flop is one, if the current-sensing output leads the input test signal; otherwise, it is zero. At the onset of the tuning operation, the counter, which controls the tuning voltage, is reset to g_{m2}(min) and the output of the flip-flop is one, which starts the count. The bias current of g_{m2} is gradually increased as the counter counts up, consequently raising g_{m2}, until the phase difference is eliminated, at which point the counter stops and g_{m2} is set:

$$\tan^{-1}\left(\frac{2\pi f_{ref} L}{R_L}\right) = \tan^{-1}\left(\frac{2\pi f_{ref} C}{g_{m2}}\right) \tag{3.6}$$

or

$$\frac{L}{R_L} = \frac{C}{g_{m2}}. \tag{3.7}$$

Figure 3.11 illustrates the phase response of V_{Sense} and V_1 for various g_{m2} values, and how their difference is eliminated once a proper value for g_{m2} is reached.

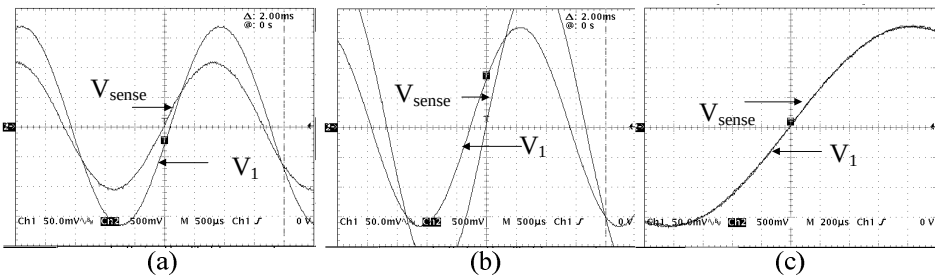


Figure 3.11—Output V_{sense} versus reference V_1 phase response at a f_{ref} of 300Hz with (a) maximum, (b) minimum, and (c) tuned g_{m2} values.

The counter *clock* frequency (Figure 3.10) should be several times lower than the sinusoidal reference frequency to allow the circuit to reach its steady-state operation after each new bias current setting, as the bias current is incremented by the counter. For reliability and robustness, a clock frequency of $f_{ref}/8$ was used, which, theoretically,

allows the system to reach 99.96% of its steady-state value before the onset of the following clock signal (i.e., after eight time constants).

A decoupling capacitor $C_{decouple}$ is used to filter out the DC part of the signal, thereby canceling the offset effects associated with the g_m cells. The phase lag incurred by the low-offset amplifier is negligible, which implies that the bandwidth of the amplifier must be greater than the frequency of the tuning reference signal (e.g., $f_{3dB\text{-}amp}$ is greater than $50f_{ref}$ for a 1° phase error). Frequencies f_{ref} and $f_{3dB\text{-}amp}$ are therefore selected to be 300 Hz and 15 kHz, respectively. For a constant gain of 20 V/V, this results in a unity-gain-bandwidth product of 300 kHz for the amplifier, which is feasible. Depending on the number of bits used for tuning, a few hundred milliseconds may be required for the tuning operation to be completed. A successive binary search, instead of the implemented linear search, would substantially reduce the time required to tune the circuit.

Calibration Phase

In the calibration phase (Figure 3.12), the gain of the low-pass filter is adjusted against the current running through a reference resistor. A constant reference voltage forces a constant DC current through the inductor, assuming R_{ref} is much greater than R_{ESR}. A low-offset amplifier (the same amplifier used in the tuning phase) amplifies the voltage across the inductor, and after resetting the counter, g_{m1} is adjusted with each count, from its minimum to its maximum value, while holding g_{m2} constant, which keeps the bandwidth constant. The counter stops when V_{Sense} reaches reference target voltage V_C, resulting in

$$V_C = I_{ref} R_L k \left(\frac{g_{m1}}{g_{m2}} \right); \tag{3.8}$$

therefore, the estimated current during normal operation is

$$V_{Sense} = I_L R_L \left(\frac{g_{m1}}{g_{m2}} \right) = I_L \left(\frac{V_C}{k I_{ref}} \right). \tag{3.9}$$

If constant $V_c/(kI_{ref})$ is defined to be 1, the current-sensing gain is 1 Ω, as in Equation 3.9.

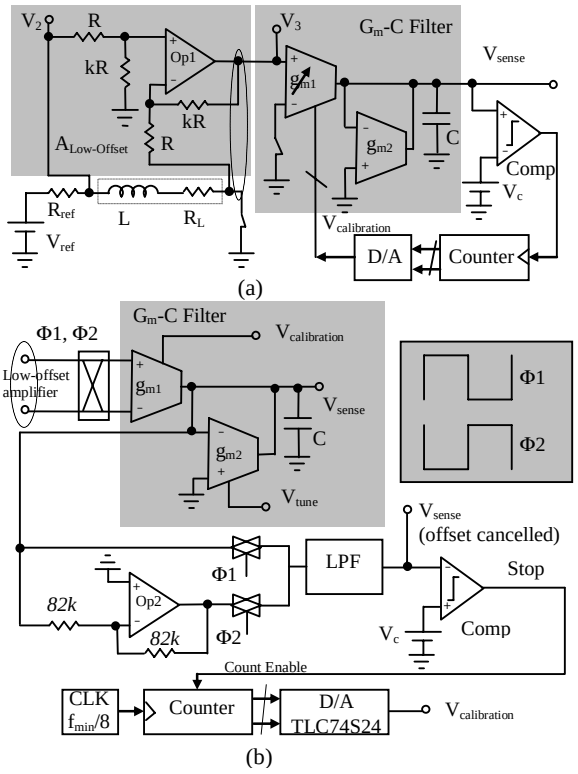


Figure 3.12—PCB prototype (a) calibration block and (b) offset-cancellation circuit.

The problem, as stated in the previous subsection, is the offset introduced by the resistor dividers, which were used for linearization. If the g_m-cell bias currents were constant, the offset would also have been constant and easily eliminated. However, the input-referred offset of the g_m-cell varies with its bias current since the offset of a differential stage is proportional to its transconductance. Thus, an offset-cancellation technique is required during the calibration period for accurate operation. The effects of variable offsets can be eliminated in the tuning phase by using a large decoupling capacitor. The same remedy cannot be used during calibration because the information needed is in the DC part of the signal.

Therefore, a chopper-stabilized offset-cancellation [53] technique was adapted for the calibration phase (Figure 3.12(b)). Another amplifier (Op2) is added to the circuit to generate an inverting output voltage. During phase **Φ**1, the output of the g_m-C filter is $A(V_{in}+V_{os})$, where V_{in} is the input voltage, V_{os} is the input-referred offset voltage, and "A" is the gain from the input to the output of the g_m-C filter. During phase **Φ**2, the g_m-C filter output is $A(V_{in}-V_{os})$. Hence, if a low-pass filter is used at the output of the g_m-C

filter, the average output is AV_{in}, which has no offset errors.

3.2.3. Experimental Results

A 20 µH inductor with 45 mΩ of ESR was used and the desired current-sensing gain was set to 0.5 Ω (i.e., $I_L = V_{sense}/0.5\ \Omega$). The system was tuned and calibrated, first by using the discussed tuning and calibration algorithms and normal operation was then tested.

The family of curves for the measured DC currents versus the actual DC values is shown in Figure 3.13. Filter gain was varied by adjusting g_{m1} bias current, and the estimated current (filter output) for current loads from 0 A to 1 A were measured for various filter gains. The thick bold line is the targeted 0.5 V/A gain and the thin bold trace is the experimental result for calibrated g_{m1} for 0.5 V/A gain. The calibrated curve follows the targeted trace from 0 A to 0.1 A. Then it slightly separates from ideal curve as the current rises from 0.1 A to 0.2 A. The difference between the calibrated and targeted curves becomes a constant offset change (about 18 mV) for the remaining 0.2 A to 1 A range, where the 0.2 A current corresponds to the boundary of the buck converter's continuous- and discontinuous-conduction modes (CCM and DCM). This effect is a systematic offset caused by the nonlinearity of the g_m cells.

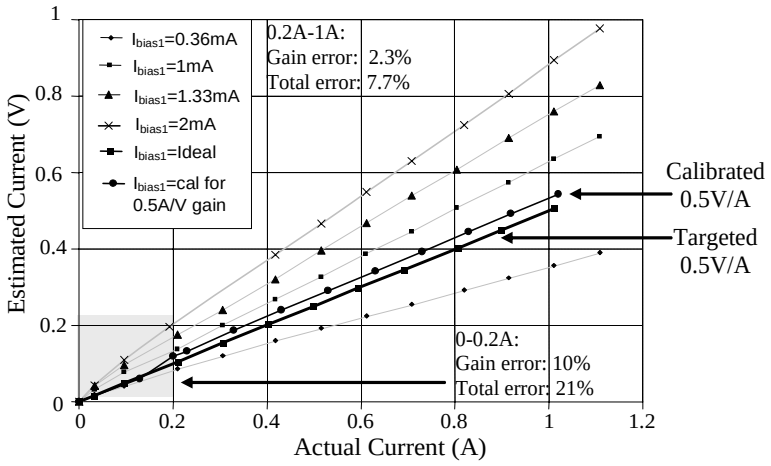


Figure 3.13—PCB prototype family of curves of measured current for various g_{m1} settings. The thick bold trace is the targeted 0.5 V/A gain and the thin bold trace is the calibrated gain.

The systematic offset essentially results because of the common-mode range dependence of the transconductance of the g_m cells. The signal at the g_m-C filter input during normal operation is rectangular by nature. For a buck converter operating in CCM, the voltage at the junction of the power switches is V_{in} when the high-side switch is on, and zero when the low-side switch is on. On the other hand, the voltage at the output of the converter (V_{out}) is approximately constant because the output ripple voltage is significantly smaller. Therefore, the common-mode range of the filter is wide enough to cause transconductance errors, which ultimately distort the output sense voltage (V_{sense}). Changing g_{m1} to $g_{m1}+\Delta g_{m1}$ when the input voltage changes from zero to V_{in} changes the output sense voltage by

$$V_{os\_sys} = \Delta g_{m1}\left(\frac{1}{g_{m2}}\right)D(V_{in} - V_o) \tag{3.10}$$

or equivalently

$$V_{os\_sys} = \left(\frac{\Delta g_{m1}}{g_{m1}}\right)\left(\frac{g_{m1}}{g_{m2}}\right)D(V_{in} - V_o), \tag{3.11}$$

where D is the duty cycle of the rectangular signal. The systematic offset is considerable if the gain (g_{m1}/g_{m2}) and nonlinearity ($\Delta g_{m1}/g_{m1}$) are high. For the case of the prototype, where g_{m1}/g_{m2} is 12.5, V_{in} is 5 V, V_{out} is 3.3 V, D is 66%, and $\Delta g_{m1}/g_{m1}$ is 0.15% for the resistor division factor of 820, Equation 3.11 predicts 21 mV of offset, which is close to the experimental value of 18 mV. Cells with higher linearity can be designed to limit the systematic offset to a minimum value, but at the cost of more complex g_m cells. For DCM buck converter operation (e.g., current below 0.2 A, as in Figure 3.13), a lower systematic offset occurs because of the oscillations at the positive inductor port during the high-side switch "on" time. Therefore, DC accuracy is a function of both gain error resulting from calibration loop limitations and systematic offset error due to g_m-cell non-linearity. Although, the total error is the sum of gain error and systematic offset errors, the systematic offset error is not inherent and can be eliminated using higher performance circuits. In Figure 3.13, the measured current gain calibrated for 0.5 V/A gain (thinner bold trace) has 10% gain error from 0 A to 0.2 A and 2.3% gain error from 0.2 A to 1 A. The total error, including systematic offset error, is 21% at 0.2 A and 7.7% at 1 A.

A continuous real-time measurement of the inductor current is another important goal of the proposed technique. The experimental continuous output ripple current response of the circuit matches the actual ripple current with an AC error of less than 5%, as shown in Figure 3.14. The actual inductor current was derived from the output ripple voltage, since the relatively large ESR (0.15 Ω) of the output capacitor mostly defines the ripple voltage across it, which is linearly proportional to the inductor ripple current. The reference current can also be measured using a relatively high series sense resistor (e.g., 0.1 Ω, the traditional current-sensing method).

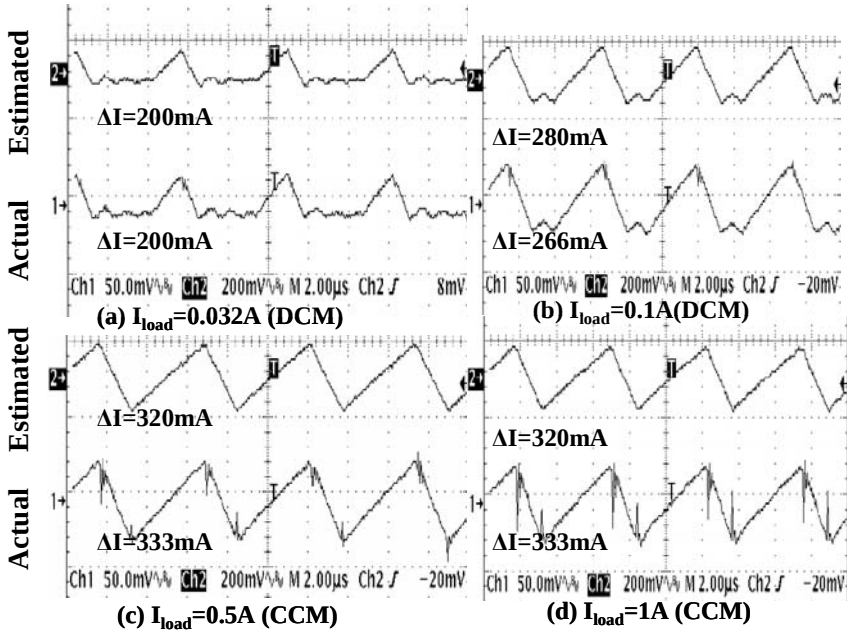


Figure 3.14—PCB prototype estimated and actual AC inductor currents during normal operation and under various loading conditions.

3.3. Integrated Circuit Challenges

Several issues limit the use of the low frequency tuning implemented in the PCB prototype in a fully integrated circuit. First, generating an on-chip sinusoidal test signal is difficult, if not impractical. Second, implementation of a high-pass filter with a cut-off frequency of around a few hundred Hertz requires high value resistors and capacitors, and consequently a large die area. Third, the effective inductance at low frequencies, which is

what is being measured in low frequency tuning, is different from the effective inductance at normal operating conditions where the actual switching frequency is significantly higher. Fortunately, all these issues are resolved with high frequency tuning where a triangular high frequency test signal is used. The required high-pass filter cut-off frequency is increased to about 50 kHz, and the tuning frequency is close to the switching frequency of the converter.

Simple block diagrams of the high frequency tuning and calibration circuits are shown in Figure 3.15 and Figure 3.16, respectively. The tuning loop consists of a test-signal generator, an adjustable g_m-C filter, a preamplifier with gain K, a comparator, a DC-removal unit, and a counter. The calibration circuit consists of the same blocks except for the DC-removal unit. During the tuning phase, a triangular current at switching frequency is forced into the inductor. At these high frequencies, the inductor's R_{ESR} is considerably smaller than inductor impedance ($L\omega$) and g_m-C filter capacitor impedance ($1/C\omega$) is much lower than resistor R. As a result, at high frequencies, the transfer function from the inductor current to the output sense voltage becomes

$$V_{Sense\_Tune} = \left(\frac{g_m L}{C}\right) I_L . \tag{3.12}$$

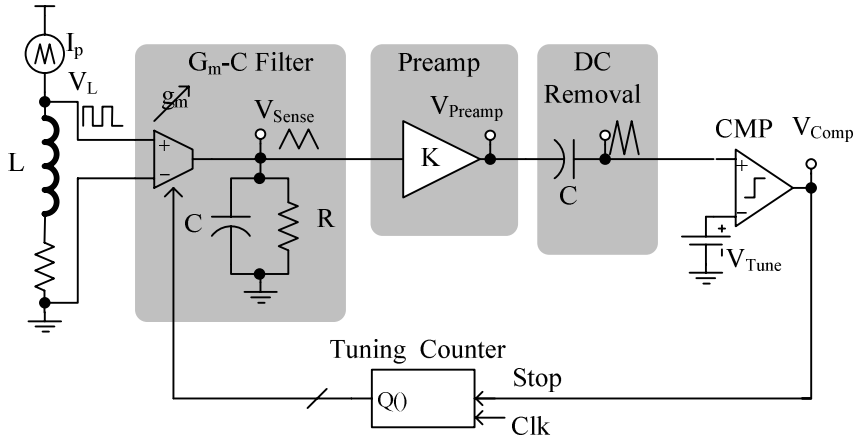


Figure 3.15— High frequency tuning block diagram suitable for integration.

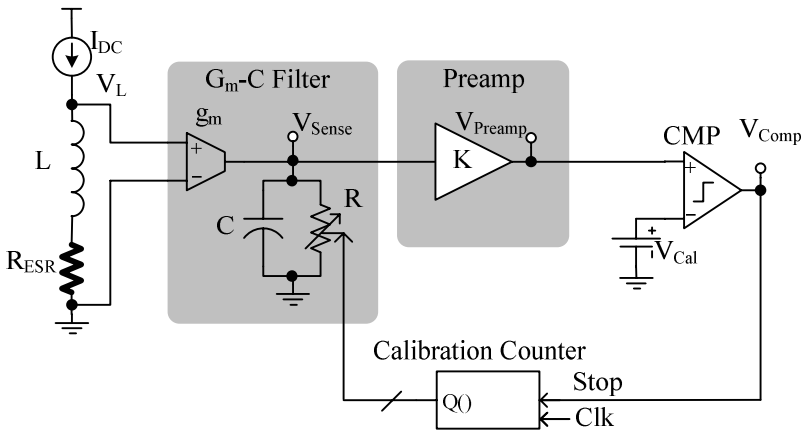


Figure 3.16—Calibration block diagram suitable for integration.

Consequently, the output of g_m-C filter is a triangular signal similar to the test current. The signal at the output of the g_m-C filter is amplified with a gain stage, and its AC part is compared to a constant voltage (V_{Tune}). Therefore, the output of the comparator, CMP, is activated if the peak value of the triangular signal at the output of the preamplifier exceeds V_{Tune}. The loop is responsible for adjusting the transconductance g_m such that the preamplifier's output peak voltage is V_{Tune}, or equivalently,

$$\left(\frac{g_m L}{C}\right) K I_p = V_{Tune}\,, \tag{3.13}$$

where K is the preamplifier gain and I_p is the peak value of the triangular test signal. The preamplifier is used to amplify the output of the current-sensing filter to a suitable value for processing, since test currents during start-up are considerably than the inductor current during normal operating conditions, when switching regulator is working.

The tuning loop regulates as follows: A clock gradually increments the counter, the outputs of which control the value of transconductance g_m via a network of switches. Therefore, at each clock increment, the value of transconductance g_m increases. The tuning phase starts with a reset of the counter that sets transconductance g_m to its lowest value. While g_m is lower than the targeted value, comparator CMP's output is disabled. Eventually, g_m becomes large enough that the peak voltage of signal at the output of the preamplifier exceeds V_{Tune}. Then, the output of comparator CMP trips and stops the counter at the targeted transconductance g_m value the one that satisfies Equation 3.12.

In the calibration phase, which starts once the tuning phase is completed, a DC

current is forced into the inductor (Figure 3.16). The resulting voltage across the inductor and the output of g_m-C filter are DC signals. The g_m-C filter output is then amplified through preamplifier Preamp and the result is forced to equal to constant voltage V_{Cal} through the feedback loop, or equivalently,

$$(R_{ESR} I_{DC})(g_m R)K = V_{Cal}, \tag{3.14}$$

where I_{DC} is the calibration DC test current and R is the g_m-C filter resistor.

A procedure similar to that discussed in tuning is applied to the calibration loop, with a counter controlling the value of resistor R. If calibration and tuning voltages and test currents are designed to satisfy

$$\frac{V_{Tune}}{I_p} = \frac{V_{Cal}}{I_{DC}}, \tag{3.15}$$

the g_m-C filter is properly adjusted to measure inductor current. The filter's cut-off frequency 1/RC becomes equal to the inductor's bandwidth R_{ESR}/L as depicted in Equations 3.13, 3.14, and 3.15, and current-sensing gain α is consequently set to

$$\alpha = \frac{V_{Cal}}{KI_{DC}}. \tag{3.16}$$

After the calibration phase is finished, the switching regulator resumes normal operation and the g_m-C filter measures the inductor current accurately (i.e., $V_{Sense} = \alpha I_L$).

The block diagram of the proposed integrated circuit proposed is shown in Figure 3.17. The chip includes an adjustable g_m-C filter, tuning and calibration loops, and a PWM current-mode controller for a buck switching regulator (Figure 3.17(a)). The DC-DC converter is used as a test bed to evaluate the precision and noise level of the current-sensing circuit. The chip includes a triangular-signal generator for tuning, a test-current generator (Figure 3.17(b)) to force the test current into the inductor at start-up, and logic (i.e., digital core) to control the transition from tuning to calibration and from calibration to normal operation (Figure 3.17(c)). Housekeeping blocks such as a voltage reference and bias-current generator are also included for stand-alone operation.

As with most of switching regulator circuits, the chip uses a few external components. These off-chip components include power inductor L and capacitor C for the power stage of buck converter and a controller compensation network (R_a, R_b, and

C_{comp}) as shown in Figure 3.17. Power switches M1 and M2 can be implemented off-chip or on-chip, but the latter requires a large die area. For state-of-the-art fabrication technologies, on-chip MOSFET switches rated up to 2 A are technically and economically justified.

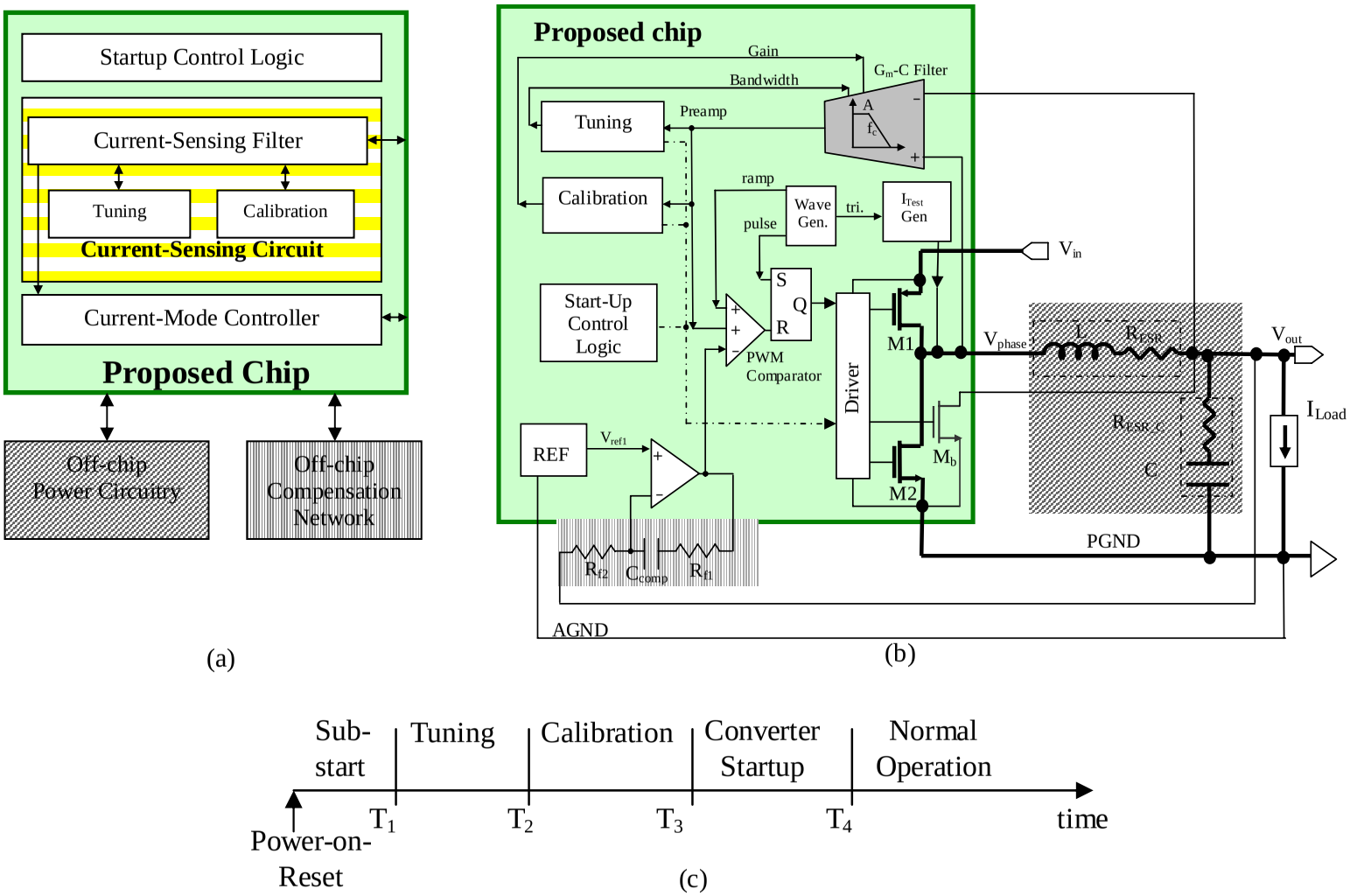


Figure 3.17—(a) Simplified and (b) detailed block diagram of the proposed chip, and (c) its start-up timing sequence.

Although the proposed technique uses self-calibration to adjust the on-chip filter to the off-chip inductor, the range of inductors that can be used with the proposed system is determined by programming bandwidth and gain range of the g_m-C filter. High-performance switching regulators and current-sensing circuits are especially important in portable applications, where every bit of battery power must be saved. A targeted inductor range of 2 μH to 6 μH is selected, since the range is typical for inductors used in these high frequency high-performance DC-DC converters. Based on the PCB prototype results, an accuracy of ±10% for the integrated prototype of the current-sensing technique was found feasible, which is far superior to available techniques such as basic filter, sense-FET, and MOSFET-R_{DS}. A current-sensing gain of 0.5 V/A was also found to be appropriate for these applications where load current is typically below 1 A. Key specifications of the current-sensing circuit are provided in Table 3.1. Similarly, the specifications of the DC-DC converter are given in Table 3.2.

Table 3.1—Proposed current-sensing module specifications.

Current-Sensing Specifications		
Spec. Comp.	**Target**	**Notes**
$R_{gain} = V_o/I_L$	0.5 V/A	0.5 V for 1 A max current
Bandwidth for 1 MHz switching frequency	8 MHz	Less than 1% AC error Stability of current loop
R_{gain} Accuracy	<±10%	For high-performance control schemes
Start-up-Time	<1 s	<50 ms for VRM9, system dependent
Supply Voltage, V_{DD}	2.7 V – 4.2 V	Li-Ion battery
Load Current, I_{Load}	0 A - 1.1 A	Cell-phone/ PDA/LED driver
L Range	2 μH – 6 μH	Mainstream type
R_{ESR} Range	0.012 Ω - 0.188 Ω	Mainstream type
ICMR (In+)	-1 V - V_{DD}	Buck converter phase node
ICMR (In-)	0 V - V_{DD}	Buck converter output node
C_{out}	2 pF	Current-mode PWM comparator input cap.
Switch_EN Threshold	$V_{DD}/2$	CMOS
C_{in} (In+)	<10 pF	g_m-C filter input stage
C_{in} (In-)	<10 pF	g_m-C filter input stage
R_{in} (In+)	>20 kΩ	<100 μA current
R_{in} (In-)	>20 kΩ	<100 μA current

Table 3.2— Switching regulator specifications.

Converter Type	Buck (step-down) converter
Input Voltage	2.7 V – 4.2 V (Li-ion battery)
Output Voltage	1.5 V (0.25 μm CMOS technology)
Control Technique	PWM current-mode control
Output Current	0 – 1 A Cellular-phone and PDA processor
Output Voltage Accuracy (DC + Transient)	5% (±45 mV)
Efficiency	>80% at full load (1 A)
Switching Frequency	1 MHz

SUMMARY

This chapter proposed a lossless and accurate current-sensing technique for DC-DC converters that is insensitive to the power inductor selected by end users. The technique introduced low and high frequency tuning and calibration schemes, two ways that measure the off-chip inductor's inductance and ESR during start-up and adjust an on-chip current-sensing filter accordingly. The PCB implementation of the low frequency tuning and calibration circuits using discrete components was then built, evaluated, and presented to gauge the feasibility of the proposed self-calibrating technique. Finally, an integrated circuit (IC) consisting of the self-calibrating current-sensing circuit with the high frequency tuning and calibration and a current-mode-controlled PWM buck converter as a test bed was proposed; its top-level specifications were derived to meet the requirements of high-performance high-frequency switching regulators for portable applications. The next chapter discusses the performance of the proposed circuit, provides system-level design guidelines, and derives the specifications of the various supporting sub-blocks to ultimately achieve ±10% accuracy.

CHAPTER 4

ACCURACY

As with any electronic system, operating-point conditions (e.g., temperature) and circuit non-idealities will affect the performance of the proposed current-sensing technique. The inductor component inductance and ESR are only measured during start-up, but changes in temperature, inductor current, and switching frequency during operation affect the model parameters of the inductor and cause errors because tuning and calibration are only performed during the start-up. Additionally, during the tuning and calibration phases, circuit non-idealities such as offset, gain, and quantization errors result in incorrect settings for filter bandwidth and gain. This chapter defines metrics for accuracy of the current-sensing circuits; discusses various error sources that limit the performance of the proposed self-calibrating filter; quantifies the effects of these errors on overall accuracy of current sensing; identifies the dominant error sources; and derives the circuit block specifications to achieve the targeted ±10% accuracy performance.

4.1. Inductor Model

Similar to other power electronic applications [54], an ideal inductance in series with an ESR resistor is used as the power inductor model in the proposed technique. In practice, a more advanced model is required to model inductor behavior between low frequencies (10 kHz) and very high frequencies (1 GHz) [55-59], as shown in Figure 4.1, where R_p is the resistance to model inductor core losses, C_p is the parasitic capacitance across the inductor, and Z(s) is the ESR–frequency-dependent section, because of the skin effect. In the advanced model, the parasitic capacitor, C_p, is included because of capacitance between wire windings and the inductor leads. The resonance of this parasitic capacitor with the inductor changes the effective inductance of the inductor with frequency and reduces inductor inductance above the resonance frequency (Figure 4.2). However, for power inductors, the operation frequency (i.e., the switching frequency) is limited to low frequencies (10 kHz to 1 MHz), which is usually more than a decade lower than the self-resonant frequency of the power inductor, therefore the parasitic capacitor can be neglected in power inductor models.

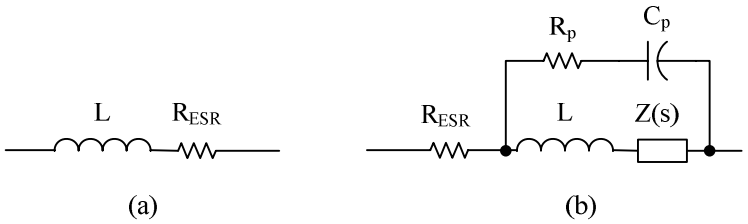


Figure 4.1— Inductor models: (a) simplified and (b) advanced.

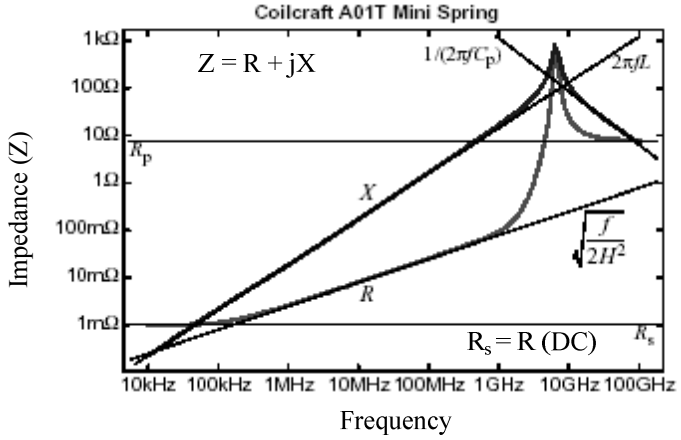


Figure 4.2—Impedance characteristics of typical inductors. The non-idealities

The skin effect causes the high-frequency current to flow close to boundaries and not in the center of the conductor. At low frequencies, the current flows in the whole conductor cross section, but at high frequencies, the current flow is concentrated mostly at conductor boundaries. It has been shown that the inductor ESR increases proportionally to the square root of the frequency at frequencies in which the skin depth is less than the conductor radius [58-59]. Fortunately, the current-sensing transfer function is insensitive to ESR value at high frequencies. The current-sensing transfer function (Figure 4.3) for a frequency-dependent ESR is

$$V_{Sense} = g_m R\left(\frac{R_{ESR}(s)+sL}{1+sRC}\right)I_L, \tag{4.1}$$

where L is the inductance and R_{ESR} is the ESR of the power inductor and R, C, and g_m are components of the g_m-C filter. Power inductors exhibit high Q values (Q>50) because of their ferromagnetic cores. Therefore, at frequencies high enough to cause the skin effect to exhibit itself, $R_{ESR}(s) << 2\pi fL$ and $1 << CR$, hence:

$$V_{Sense} = g_m\left(\frac{L}{C}\right)I_L, \tag{4.2}$$

which is independent of the ESR value. Therefore, the change in ESR at high frequencies due to the skin effect does not affect the current-sensing technique. To verify this claim, the effect of the skin effect on three arbitrarily chosen power inductors was investigated. Each inductor ESR was measured using an Agilent 4192A network analyzer over frequency, and the impact of the skin effect on the current-sensing technique was calculated over frequency by using

$$\frac{V_{sense}}{I_L} = \left|\frac{R_{ESR}(f) + j\omega L}{1 + j\omega RC}\right|, \tag{4.3}$$

where R and C are selected such that $L/R_{ESR\_DC} = RC$, and (g_mR) is selected to be $1/R_{ESR\_DC}$. Any error caused by the skin effect will alter the trans-impedance in Equation 4.3 from unity. For these experiments and for frequencies up to 10 MHz, the impact of the skin effect on the transfer function was less than 1% in all three inductor cases; therefore the skin effect can be neglected from the power inductor model.

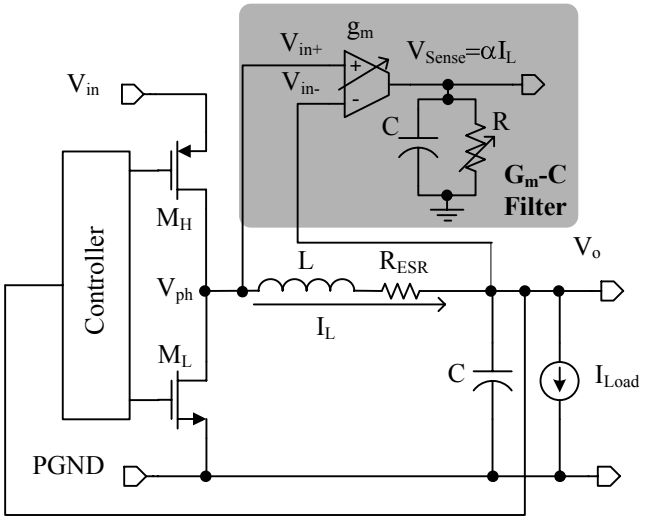


Figure 4.3—Proposed current-sensing technique as applied to a buck DC-DC converter.

The inductance model is also a function of frequency in the advanced model because of parasitic capacitance C_p. The inductance of three power inductors was measured at different frequencies using an impedance analyzer that measures the inductor

characteristic at each frequency, assuming a simplified inductance in series with the resistance model. The results are given in Figure 4.4, which shows that the effective inductance can vary up to 10%, if operation frequency changes by three decades. Therefore, to reduce the error due to inductor change with frequency, the inductance should be measured around normal operating frequency, which suggests an advantage for high-frequency tuning compared to the low-frequency tuning scheme.

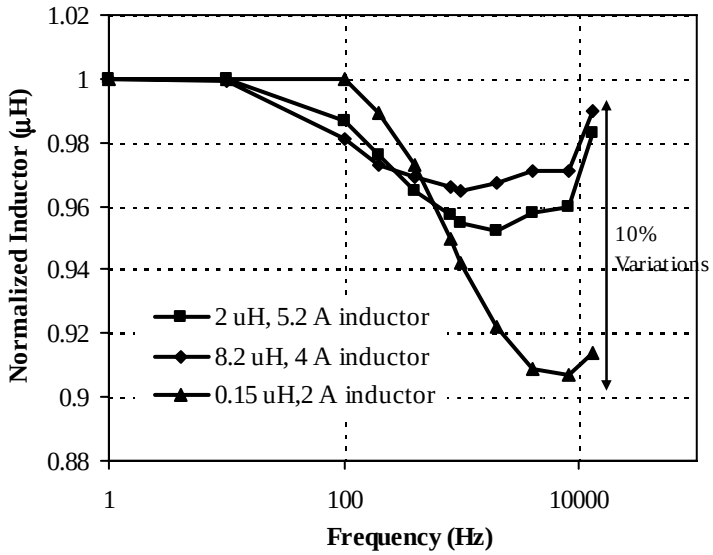


Figure 4.4—Typical power inductor inductance variations with frequency.

The inductance value also depends on the inductor current. Ferrite and other high permeability materials that are used in inductor cores exhibit flux density saturation (i.e., the flux density (B) does not increase further with increasing magnetic field intensity (H) after a maximum flux (B_{max}) is reached). Core saturation reduces the inductance at high currents compared to that at low inductor currents where the core is not saturated. A DC-DC converter is not usually designed to work with much core saturation (not more than 20% inductance drop), since working in saturation increases current ripple at high load currents and reduces power efficiency. Usually power inductors are rated for a maximum current such that the inductance decreases to between 90% and 95% of its low-current

value. Consequently, the proper choice of power inductor can eliminate the current-sensing error due to saturation.

Both inductance and ESR resistance vary with temperature. The inductance temperature coefficient of ferrite cores is from 200 ppm/°C to 800 ppm/°C, depending on the operating temperature and power magnetic core material. For example, unshielded bobbin inductors are less sensitive to temperature changes than shielded versions, since their effective air gap is larger. The temperature coefficient of the inductors decreases as temperature rises toward the Curie temperature, a temperature at which electromagnetic material loses its electromagnetic property. The Curie temperature of ferrite is around 300°C to 500°C. The inductor behavior over the temperature range was measured for a typical power inductor, and the result is given in Figure 4.5. The measured variation in inductor value due to an 80°C temperature change is within ±10% of its value.

Finally, the most significant change to the inductor model parameters due to operating conditions is the variation of ESR with temperature. The power inductor wiring is mainly copper, with a resistance temperature coefficient of 3900 ppm/°C. The targeted temperature range for power supplies is from -40°C to 85°C. Therefore, temperature variations can result in ±25% error in the proposed current-sensing circuit if the calibration is performed at room temperature (27°C). Nevertheless, the ESR temperature coefficient is almost constant over a wide range of temperature, and the effect of temperature on the inductor ESR can be compensated through circuit techniques, if temperature is sensed. These techniques will be discussed in Chapter 6.

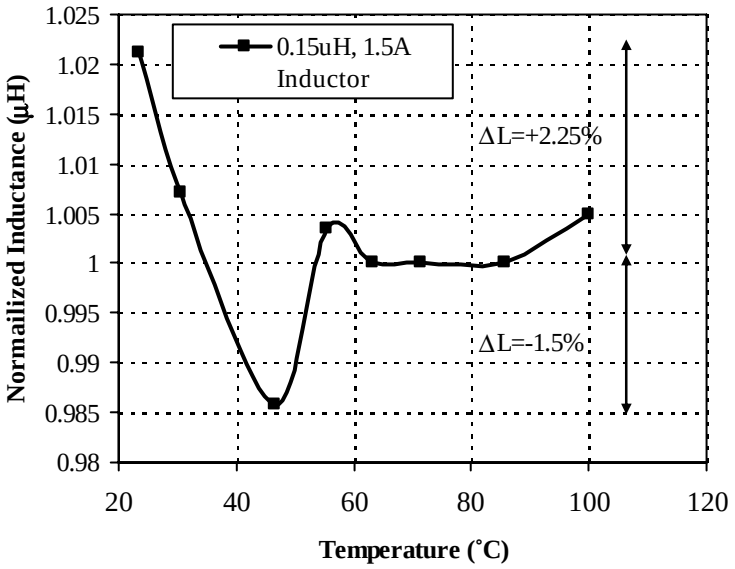


Figure 4.5—Typical power inductor inductance variations with temperature.

4.2. Errors

Inductor current in switching regulators consists of DC and triangular AC components, as illustrated in Figure 4.6(a). Various problems can affect the current-sensing transfer function differently and may cause errors in the estimated value of the AC or DC components. When the filter pole is not at exactly the same location as inductor zero, it changes the AC triangular peak-to-peak value, causing AC errors, as illustrated in Figure 4.6(b). If the filter bandwidth is higher than inductor zero, the peak-to-peak value of the ripple current increases; and if filter bandwidth is less than inductor zero, the peak-to-peak value of the ripple current decreases. Nevertheless, because of the nature of the filter technique, phase shift is prohibited as a result of an AC error. In the proposed technique, tuning loop errors are the source of AC gain errors.

DC errors (Figure 4.6(c)) are caused by g_m-C filter offset or calibration loop errors. The g_m-C filter offset can be categorized as both a random offset due to circuit mismatch and a systematic offset due to non-linearity. A detailed discussion is provided later in this chapter. Moreover, the calibration loop error sets g_mR to an incorrect value and causes DC gain errors. The effect of these errors on the current-sensing DC characteristics is shown in Figure 4.7.

To quantify the accuracy of current-sensing circuits, we define the current-sensing error at each inductor DC current value as the weighted addition of DC error and AC error. The current-sensing circuit AC and DC errors are defined as

$$\text{Error(AC)} = \frac{\Delta\alpha_{AC}}{\alpha_{AC}} \equiv \frac{\Delta I_L\,(\text{Estimated}) - \Delta I_L\,(\text{Actual})}{\Delta I_L\,(\text{Actual})} \tag{4.4}$$

and

$$\text{Error(DC)} = \frac{\Delta\alpha_{DC}}{\alpha_{DC}} \equiv \frac{I_{L\_DC}\,(\text{Estimated}) - I_{L\_DC}\,(\text{Actual})}{I_{L\_DC}\,(\text{Actual})}, \tag{4.5}$$

respectively, where α_{AC} is the current sensor AC gain, α_{DC} is the current sensor DC gain, ΔI_L is the inductor ripple current, and I_{L_DC} is the inductor DC current. The total error at each DC current level is defined as

$$\text{Error(Total)}\Big|_{I_{L\_DC}} \equiv \left(\frac{I_{L\_DC}}{I_{L\_DC} + \Delta I_L}\right)\text{Error(DC)} + \left(\frac{\Delta I_L}{I_{L\_DC} + \Delta I_L}\right)\text{Error(AC)}. \tag{4.6}$$

Intuitively, Equation 4.6 gives more weight to DC errors at high loads where $I_{L\_DC} >> \Delta I_L$ and increases the weight of AC errors at low loads when ΔI_L becomes comparable to I_{L_DC}. For a buck converter, the total error at full load, where $I_{L\_DC} = I_{Load\_max}$, and the boundary of continuous and discontinuous conduction modes (CCM and DCM), where $I_{L\_DC} = \Delta I_L$, can be used as indices to gauge the accuracy of a current-sensing technique.

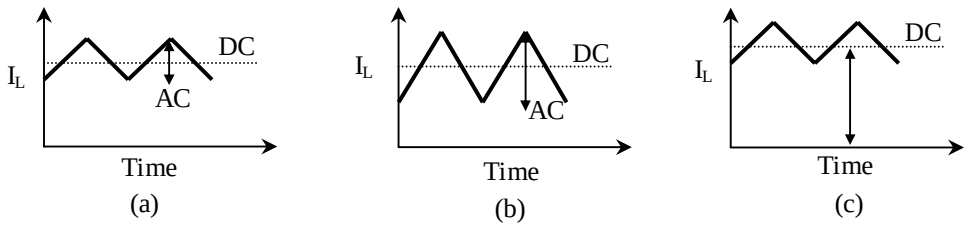


Figure 4.6—Sensed inductor current with (a) no errors, (b) AC (ripple) errors, and (c) DC errors.

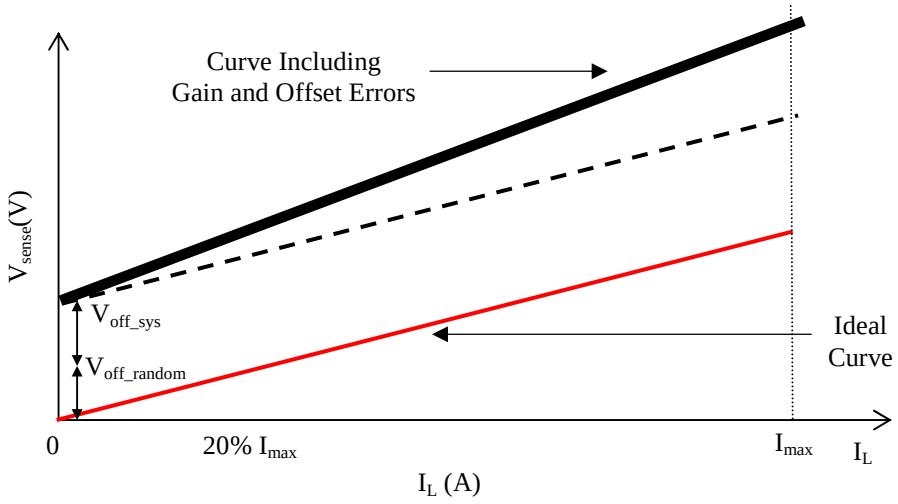


Figure 4.7—Effects of offset and gain errors on DC measurements.

4.2.1. Operating-Point Errors

The errors related to operating point are ESR and inductance value changes during normal operation from their start-up values. An ESR change after start-up constitutes a DC gain error and a change in inductance originates as an AC error. The effects of operating-point conditions on ESR value were discussed in Section 4.1 and are summarized in Table 4.1.

The significant errors are ESR change with temperature, inductance change with inductor current, and inductance change with operation frequency change, but all are limited or can be compensated for by proper design. The design can compensate for ESR change with circuit techniques if temperature is sensed. The proper selection of inductor current ratings can prevent inductor from operating in the core saturation region, and selecting a high-frequency tuning scheme with a tuning-signal frequency close to normal operating frequency can eliminate the errors caused by a tuning frequency very different from normal operating frequency.

Table 4.1—Effects of temperature, operating current, and operating frequency on current-sensing circuit.

Error Source	Nature of Error	% Error	Systematic/ Random	Predictability (2)	Compensation
R_{ESR} vs. Temperature (T = -40°C to 85°C)	Copper Temp. Co. (3900 ppm/°C)	DC: ±25%	Systematic	High	Yes
L vs. I_L	Core Saturation	AC: 0-20% DC: 0-4%	Systematic	Low	No, Proper Selection of Inductor
L vs. Temperature (T = -40°C to 85°C)	Magnetic Temp. Co. (200-800 ppm/°C)	AC: ±1.25%-±5%	Systematic	Medium	Maybe
R_{ESR} vs. Frequency	Skin Effect	AC: 0 DC: <1%	Systematic	Medium	No
L vs. Frequency	Parasitic Capacitor (1-3% per decade)	AC: <1% DC: 0	Systematic	Low	No, High Freq. Tuning
R_{ESR} vs. I_L (1)	-	-	-	-	-

(1) This effect is considered in combination with R_{ESR} versus temperature.
(2) Predictability means how an IC designer can predict and compensate the error source during the design cycle.

4.2.2. Random Offsets

The g_m-C filter random offset reduces the accuracy of the current-sensing circuit especially since the DC value of voltage across the inductor is very low even in normal operating conditions. For example, for an ESR value of 50 mΩ, a typical value for power inductors with current ratings of 1 A to 4 A, the voltage across the inductor at 1 A is 50 mV. Therefore, a 10 mV offset at the input of g_m-C filter constitutes a 20% error.

4.2.3. Systematic Offsets

The nonlinearity of g_m-C filter also constitutes a DC error at the output of the filter, which can be modeled by a systematic offset at the converter input. The effect, which was observed in the prototype measurements, can be analyzed and quantified as follows: The signal at the g_m-C filter input during normal operation is a rectangular signal. For a buck converter operating in CCM, the voltage at the junction of power switches is V_{in}, when the high-side switch is on, and zero, when the low-side switch is on (Figure 4.3). The voltage at the converter output is V_o, which is approximately constant if

the output ripple is assumed to be small. Since the average voltage across the inductance is zero in steady-state operation,

$$D\,(V_{in}-V_o-V_R)-(1-D)\,(V_o+V_R) = 0, \tag{4.7}$$

where D is the duty cycle and V_R is the average voltage across the inductor ESR; hence:

$$D = \frac{V_o + V_R}{V_{in}}. \tag{4.8}$$

The average sense voltage is

$$\langle V_{Sense} \rangle = \left((g_m R)_{@(V_{in}-V_o)} D(V_{in} - V_o)\right) - \left((g_m R)_{@V_o} (1-D) V_o\right), \tag{4.9}$$

where $g_m|_{@x}$ is the value of g_m at input voltage x, and <x> is the time average of variable x. Ideally, the g_m value should be constant throughout the input range. However, due to the non-linearity of the simple differential pair, g_m varies with the input voltage. If $g_m|_{@(V_{in}-V_o)} = g_m + \Delta g_m$ and $g_m|_{@V_o} = g_m$,

$$\langle V_{Sense} \rangle = (g_m R) R_{ESR} I_L + (\Delta g_m R) D(V_{in} - V_o) \tag{4.10}$$

or

$$\langle V_{Sense} \rangle = (g_m R)\left[R_{ESR} I_L + \left(\frac{\Delta g_m}{g_m} \right) D(V_{in} - V_o) \right], \tag{4.11}$$

where Δg_m is the difference in g_m at the two extreme operating points, which is a function of duty cycle. Therefore, the input-referred systematic offset is approximately

$$V_{os\_Sys} = \left(\frac{\Delta g_m}{g_m} \right) D(V_{in} - V_o), \tag{4.12}$$

for all loads, while the converter is working in CCM. The systematic offset is considerable if the g_m-cell nonlinearity ($\Delta g_m/g_m$) is high. For the case of the prototype ($g_m R$ = 12.5, V_{in} = 5 V, V_o = 3.3 V, D = 66%, and $\Delta g_m/g_m$ = 0.15% for the resistor division factor of 820), Equation (4.10) predicts 21 mV of offset at the output (i.e., input-referred offset of 1.68 mV), which is close to the experimental value (18 mV). Cells with higher linearity can be designed to limit the systematic offset to a specific value, but at the price of more complex g_m cells. For DCM, a lower systematic offset is expected because of oscillations at the positive inductor port during the high-side switch “on” time, which is in accordance with experimental observations of the prototype (Chapter 3).

4.2.4. Tuning-Loop Errors

An error in tuning loop sets the tuning variable (i.e., the filter gain bandwidth) incorrectly and ultimately causes an AC error. For a case of high-frequency tuning (Figure 4.8), the tuning loop varies transconductance, g_m, until the peak signal value at the output of the g_m-C filter exceeds a predetermined value in response to a known triangular current forced into the inductor, or equivalently, at the comparator input

$$V_{Tune} = K\left(\frac{g_m}{C}L\right)I_p, \tag{4.13}$$

where g_m is the g_m-C filter transconductance; C is the filter capacitor value; K is the preamplifier gain; L is the inductor value; I_p is the peak value of the tuning triangular test current; and V_{Tune} is the tuning voltage. Errors in K, V_{Tune}, I_p, and the comparator offset can set the transconductance to an incorrect value of $g_m+\Delta g_m$ error, which is given by

$$g_m + \Delta g_m = \left(\frac{V_{Tune}C}{KLI_p}\right)\left(1+\frac{\Delta V_{Tune} - V_{os3}}{V_{Tune}} + \frac{\Delta K}{K} + \frac{\Delta I_p}{I_p}\right), \tag{4.14}$$

where ΔK is the preamplifier gain error due to mismatches and bandwidth limitations; ΔI_p is the tuning test current error; ΔV_{Tune} is the tuning reference error; and V_{os3} is the comparator offset (because of the DC removal unit, the tuning loop is insensitive to g_m-C filter offset, V_{os1}, and preamplifier offset, V_{os2}). Equivalently, the relative error is given by

$$\frac{\Delta g_m}{g_m} = \frac{\Delta V_{Tune} - V_{os3}}{V_{Tune}} + \frac{\Delta K}{K} + \frac{\Delta I_p}{I_p}. \tag{4.15}$$

Since the data is stored digitally in the counter, a quantization error, $Q_T(e)$, should be added to the tuning loop error,

$$\frac{\Delta g_m}{g_m}(\text{total}) = \frac{\Delta V_{Tune} - V_{os3}}{V_{Tune}} + \frac{\Delta K}{K} + \frac{\Delta I_p}{I_p} + Q_T(e). \tag{4.16}$$

Since the AC gain of the g_m-C filter is $\alpha_{AC} = \frac{V_{Sense}}{I_L}(AC) = \frac{g_m}{C}L$, the error predicted in Equation 4.16 anticipates the current-sensing AC error due to the tuning loop non-idealities as

$$\frac{\Delta\alpha_{AC}}{\alpha_{AC}}(\text{Tuning Loop}) = \frac{\Delta V_{Tune} - V_{os3}}{V_{Tune}} + \frac{\Delta K}{K} + \frac{\Delta I_p}{I_p} + Q_T(e)\,. \tag{4.17}$$

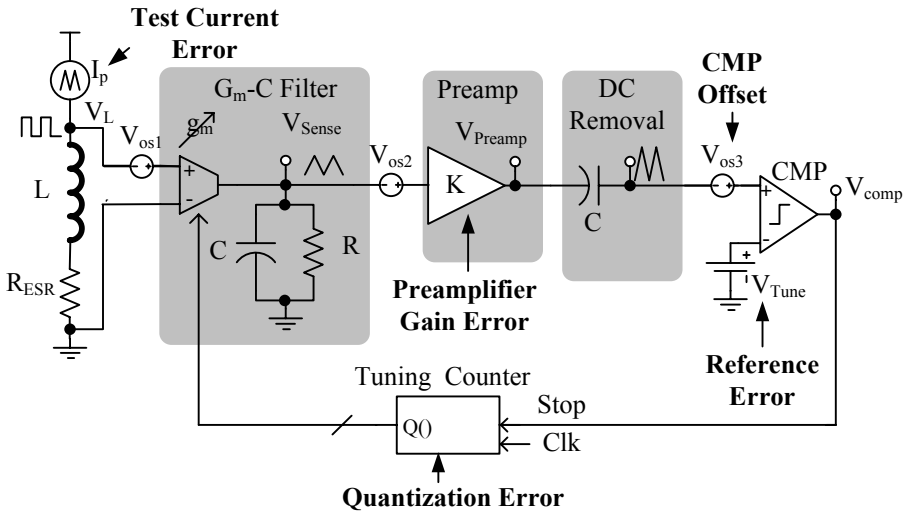


Figure 4.8—Tuning-loop error sources.

4.2.5. Calibration-Loop Errors

In contrast to the tuning loop, an error in the calibration loop sets the calibration variable (i.e., the filter DC gain) incorrectly and ultimately causes a DC gain error. For a case of high-frequency tuning (Figure 4.9), the calibration loop varies filter resistor R until the output of the g_m-C filter exceeds a predetermined value V_{Cal} in response to a known DC test current forced into the inductor, or equivalently, at the comparator input

$$V_{Cal} = K(g_m R)(R_{ESR} I_{DC}), \tag{4.18}$$

where K is the preamplifier gain; R_{ESR} is the inductor ESR value; and I_{DC} is the calibration test current value. Errors in K, V_{Cal}, I_{DC}, and offsets of the g_m-C filter, preamplifier, and comparator set the resistor R to an incorrect value of R+ΔR. To analyze the error, Equation 4.16 is revisited to consider the offset voltages, which results in

$$V_{Cal} = K\left[(g_m R)(R_{ESR} I_{DC} + V_{os1}) + V_{os2}\right] + V_{os3}, \tag{4.19}$$

where V_{os1} is the gm-C filter offset; V_{os2} is the preamplifier offset; and V_{os3} is the comparator offset. To calculate ΔR, Equation 4.17 is changed by introducing the errors, which results in

$$\frac{1}{R}\left(1+\frac{\Delta R}{R}\right)=\left(\frac{1}{\left(V_{Cal}-V_{os3}-KV_{os2}-K\left(g_m R\right)V_{os1}\right)}\right) \times Kg_m\left(R_{ESR}I_{DC}\right)\left(1+\frac{\Delta K}{K}+\frac{\Delta I_{DC}}{I_{DC}}+\frac{\Delta V_{Cal}}{V_{Cal}}\right), \quad (4.20)$$

where ΔK is the preamplifier gain error due to mismatches and bandwidth limitations; ΔI_{DC} is the error of the calibration test current; and ΔV_{Cal} is the calibration reference error. Equivalently, the percentage of calibration loop error becomes

$$\frac{\Delta R}{R}=\frac{V_{Cal}}{\left(V_{Cal}-V_{os3}-KV_{os2}-K\left(g_m R\right)V_{os1}\right)}\left(1+\frac{\Delta K}{K}+\frac{\Delta I_{DC}}{I_{DC}}+\frac{\Delta V_{Cal}}{V_{Cal}}\right). \quad (4.21)$$

As with the tuning loop, since the data is stored digitally in the counter, a quantization error, $Q_C(e)$, should be added to the calibration loop error:

$$\frac{\Delta R}{R}=\left\{\frac{V_{Cal}}{\left(V_{Cal}-V_{os3}-KV_{os2}-K\left(g_m R\right)V_{os1}\right)}\left(1+\frac{\Delta K}{K}+\frac{\Delta I_{DC}}{I_{DC}}+\frac{\Delta V_{Cal}}{V_{Cal}}\right)\right\}+Q_C(e). \quad (4.22)$$

Since g_m-C filter DC gain is $\alpha_{DC}=\frac{V_{Sense}}{I_L}(DC)=\left(g_m R\right)R_{ESR}$, the error predicted in Equation 4.22 anticipates the current-sensing AC error due to the tuning loop non-idealities as well:

$$\frac{\Delta\alpha_{DC}}{\alpha_{DC}}=\left\{\frac{V_{Cal}}{\left(V_{Cal}-V_{os3}-KV_{os2}-K\left(g_m R\right)V_{os1}\right)}\left(1+\frac{\Delta K}{K}+\frac{\Delta I_{DC}}{I_{DC}}+\frac{\Delta V_{Cal}}{V_{Cal}}\right)\right\}+Q_C(e). \quad (4.23)$$

Equation 4.23 suggests that the most dominant source of error in the calibration loop is the g_m-C filter offset. For a R_{ESR} = 50 mΩ, I_{DC} = 50 mA, g_mR=10, K=20, V_{Cal}=0.5 V and to limit the effective V_{os1} error to 1%, V_{os1} should be less than 25 μV, which is a tough specification to meet and a challenge in the design of calibration loop.

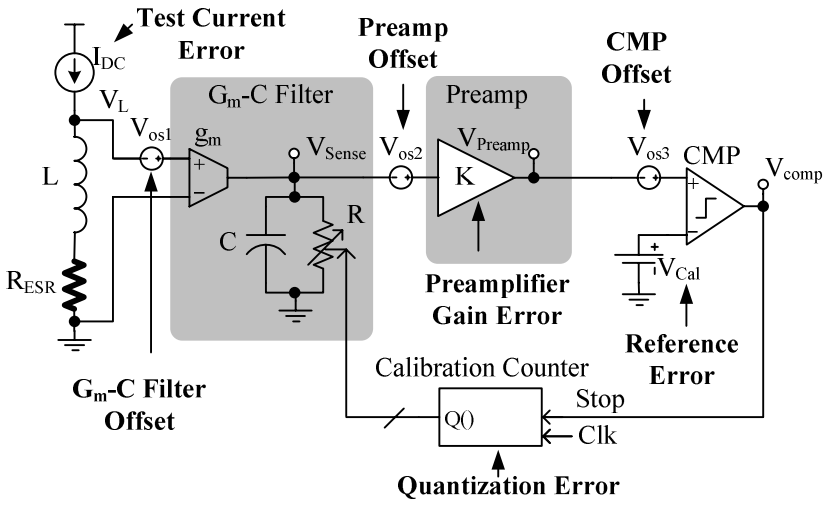


Figure 4.9—Calibration-loop error sources.

4.3. Specification Requirements

Now that all the errors contributing to the accuracy of the proposed current-sensing are identified and analyzed, it is possible to budget the allowable error to the system sub-blocks to achieve the proposed accuracy of 90% (maximum error of ±10%). The proposed AC, DC, and total current-sensing errors are calculated for full load. From 10% targeted total error, 2% is budgeted for systematic and random offsets and 7.5% is dedicated to AC and DC gain errors and ESR variations with temperature, which are the dominant operating-point errors.

In budgeting the error, systematic and random error sources are added differently. Systematic error sources are added linearly, while random error sources are added quadratically [60-62]. Assuming all sources of error are independent, the effective error (E_{Eff}) caused by *n* sources of random error and *m* sources of systematic error is given by:

$$E_{Eff} = \sum_{i=1}^{m} e_{si} + \sqrt{\sum_{j=1}^{n} e_{rj}^2}\,, \tag{4.24}$$

where e_{si} is the relative error at the output caused by the i^{th} source of systematic error, and e_{rj} is the relative 3σ error at the output caused by the j^{th} source of random error. The initial tolerance errors are considered random errors, while temperature, frequency, and current-dependent errors are considered systematic errors.

Table 4.2 summarizes the error budget of the proposed current-sensing circuit to achieve ±10% error at full load for a typical DC-DC converter (i.e., $\Delta I_L = 0.2I_{Max}$). Table

4.3 recalculates the total error for the proposed and basic filter techniques at full load and at the boundaries of CCM and DCM according to the error budget given in Table 4.2. In all, the proposed current-sensing technique improves the AC, DC, and total accuracy of basic filter technique both at full load and at the boundaries of CCM and DCM (e.g., total error at full load is reduced to ±10% from ±60%). Moreover, the filter technique accuracy is calculated assuming that the current-sensing network was designed for a known inductor, and only the initial tolerances and environmental effects are considered. Since the proposed system measures the inductor at start-up, the inductor can be selected from a range of devices, and as shown in Figure 4.10, the error is guaranteed for a range of inductance and ESR values rather than a specific inductor only.

SUMMARY

Errors in the tuning and calibration loops and changes in operating-point conditions from start-up to normal operation result in DC and AC errors in the proposed current-sensing scheme. In this chapter, these error sources were discussed and their effects on the overall error were investigated. It was shown that the change in ESR with temperature is the dominant operating-point condition that reduces the accuracy of the proposed current-sensing technique, thereby requiring correction. The offset of g_m-C filter in the calibration loop is the dominant circuit non-ideality causing significant errors and therefore should be well addressed at circuit level. The results of the investigation of error sources and their effects were applied to budget the targeted ±10% error among the proposed system sub-blocks. In the next chapter, the system design of a buck current-mode controlled switching regulator, a test bed for the proposed current-sensing circuit, is discussed before the sub-block specifications derived in this chapter are used to design the actual circuits in Chapter 6.

Table 4.2—Specification of blocks derived from error budget.

Total Error, ±10%, $\Delta I_L = 0.2I_{DC\_L}$, $I_{DC\_L} = I_{Max}$											
Offset Error ***2%***		**Gain Error** ***±7.5%***									
		AC Gain Error ***±3.125%***				DC Gain Error ***±6.25%***					
		Tuning Error ***±3.125%***				Calibration Error ***±3.125%***					Temp. Error ***±3.125%***
Random Offset: ±0.2%	Systematic Offset: ±1.8%	Tuning Current Error: ± 2%	Comparator Error: ±0.5%	Preamplifier and HP Filter Error: ±0.5%	g_m Quantization Error: ±1.5%	Calibration Offset: ±1%	Comparator Error: ±0.5%	Calibration Current Error: ±1%	Preamplifier Gain Error: ± 0.5%	R Quantization Error: ±1.5%	Temperature Error: ±3.125%
g_m-C Filter Offset Spec.	**g_m-C Filter Linearity Spec.**	**R_{ref} Accuracy Spec.**	**Comparator Offset Spec.**	**Preamplifier Bandwidth Spec.**	**g_m-cell Number of Bits Spec.**	**Calibration Offset Spec.**	**Comparator Offset Spec.**	**R_{ref} Accuracy Spec.**	**Preamplifier DC Gain Spec.**	**R Number of Bits Spec.**	**Temperature Compensation Spec.**

Table 4.3—Accuracy of the proposed self-calibrating technique versus basic filter scheme.

Error Source	% Error Initial		% Error After Compensation		Systematic /Random	Total Error[4]
	AC	DC	AC	DC		
Initial Tolerance of R_{ESR}	0	±30%		±3.12%	Random	
Initial Tolerance of L	±20%	0			Random	
Initial Tolerance of C - On-chip - Off-chip	 ±20% ±5%	 0 0	±3.12%		Random	
Initial Tolerance of R - On-chip - Off-chip	 ±20% ±5%	 0 0			Random	
R_{ESR} vs. Temperature T = -40°C to 85°C	0	±25%	0	±3.12%	Systematic	
L vs. Temperature T=-40°C to 85°C	±1-5%		±1-5%	0	Systematic	
L vs. I_L [1]	0-5%	0	0-5%	0	Systematic	
L vs. Frequency	<1%	0	<1%	0	Systematic	
R_{ESR} vs. Frequency (skin Effect)	<1%	0	<1%	0	Systematic	
Random Offset	0[5]	10%	0	0.2%		
Systematic Offset	0	0	0	1.8%		
Amplifier Gain Error	±0.1%	±0.1%	±0.1%	±0.1%	Random	
Filter Technique Error **$I_{DC}=I_{max}$, $\Delta I=0.2I_{max}$** **- On-chip** **- Off-chip**	 -39%-44% -26%-31%	 ±65% ±65%				[2,3] -61% - 63% -59% - 60%
Filter Technique Error **$\Delta I=2I_{DC}$**[6] **- On-chip** **- Off-chip**	 ±39% ±26%	 ±65% ±65%				[2,3] ±52% -±46%
Proposed Technique Error **$I_{DC}=I_{max}$, $\Delta I=0.2I_{max}$**			-9% - 14%	±%8.25		[2,3] -9% - 10%
Proposed Technique Error **$\Delta I=2I_{DC}$**[6]			±9%	±%8.25		[2,3] ±8.7%

(1) The inductor saturation only affects the accuracy at high-load currents and does not affect the accuracy at low inductor currents.

(2) The total error is calculated at maximum load current in both high-current and low-current error calculations.

(3) The total error is calculated by linear addition of systematic errors and quadratic addition of random errors.

(4) $V_{Sense} = f(ESR, L, R, C) = A\left(R_{ESR} I_{DC} + \frac{L}{RC} I_{AC}\right)$ and $\frac{\Delta V_{Sense}}{V_{Sense}} = \frac{I_{DC}}{I}\left(\frac{\Delta R_{ESR}}{R_{ESR}}\right) + \frac{I_{AC}}{I}\left(\frac{\Delta L}{L} + \frac{\Delta R}{R} + \frac{\Delta C}{C}\right)$ are used for calculating the effect of errors on the filter and proposed current-sensing techniques, where A is the amplifier gain, which is considered to be without error as compared to other error sources.

(5) Assuming ±5 mV offset for the amplifier and input voltage of 50 mV at its inputs at full load.

(6) Inductance does not saturate at low DC currents.

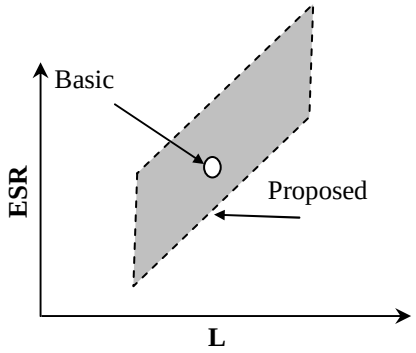


Figure 4.10— Inductor-ESR range comparison of proposed self-calibrating and basic filter techniques.

CHAPTER 5

CURRENT-MODE CONTROLLERS

A PWM buck current-mode controller has been selected as a test bed to verify the precision of the proposed current-sensing technique since current programming is sensitive to the noise on the current sensor output. This chapter begins with a brief overview on the operation of switching regulators, followed by a discussion of practical system-level issues in the design of current-mode controllers, such as compensation, large-signal stability, and transient response. The chapter concludes by providing a step-by-step procedure for designing current-mode controller systems. This procedure is used to design a prototype current-programmed buck converter for Li-Ion battery supplied portable applications (i.e., input voltage from 2.7 V to 4.2 V and load current of less than 1 A).

5.1. Types of Switching Regulators

Power-management circuits serve to supply voltage for different blocks in an electronic system from a master power source [63, 64]. For portable applications, the power source is a battery, the output voltage of which is a function of its output current and its state of charge. In the case of Li-Ion batteries, which dominate the consumer electronics market nowadays in applications such as cell phones, PDAs, and digital cameras, the battery output voltage traverses from 4.2 V when fully charged to 2.7 V when battery is completely drained. Not only most blocks require dedicated supply voltages but they may also require different voltage levels during their operation. For example, state–of-the-art processors acknowledge their appropriate voltage level to power management units depending on their processing load to minimize power consumption and ultimately to increase battery life.

Voltage regulator circuits are categorized topologically as charge pumps, linear regulators, and switching converters [63]. Charge pumps can boost input voltages; they are implemented solely with switches and capacitors, and hence, they can be fully

integrated. However, charge pumps have limited load-handling capability because capacitor values are constrained to practical values (i.e., a typical integrated charge pump can drive up to a few mA). A linear regulator, which consists of a pass transistor and an amplifier, acts as a simple resistor divider whose output voltage is controlled through linear feedback. These converters can only convert higher voltage levels to lower voltage levels, and their efficiency is low when difference between input and output voltage levels are relatively high.

Switching regulators, which are commonly called DC-DC converters in the literature, can efficiently convert supply voltage to higher or lower voltages under relatively high load currents. Although switching regulators historically were used in power electronics to transfer tens of kilowatts of power, they are relatively new in low power (i.e., 0.1 W to 100 W) applications. In consumer electronic systems, DC-DC converters are used to supply load currents from 100 mA to 100 A.

DC-DC converter power circuits consist of power switches, inductors, and at least one capacitor. The capacitor and inductor (energy-transfer elements) are almost always implemented off-chip because of their high values. The power switches can be realized on-chip, if load current is relatively low (<2A). There are several topologies for DC-DC converters [64]; buck, boost, and buck-boost converters are among the more popular topologies (Figure 5.1) [64]. The buck converter converts higher voltage levels to lower voltage levels; the boost converter converts lower voltage levels to higher voltage levels; and the buck-boost, which is the cascade of buck and boost converters, can convert the input voltage to both higher and lower output voltage levels. Although the power efficiency of a DC-DC converter can theoretically reach 100%, in practice, the conduction and switching losses degrade its efficiency to 80% to 95%.

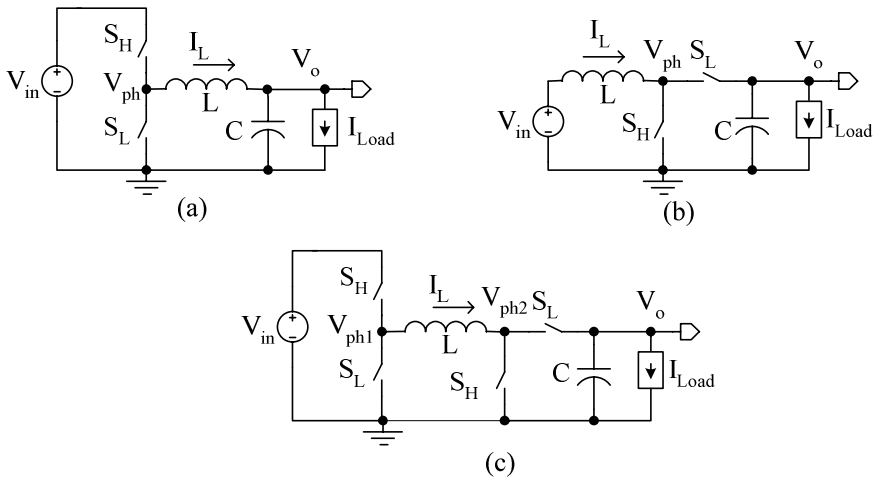


Figure 5.1—Basic DC-DC converters: (a) buck, (b) boost, and (c) buck-boost topologies.

All these converters operate using a periodic two-phase procedure. In the first phase, the inductor is charged by input voltage through a high-side switch, SH. In the second phase, the inductor current is discharged to the output capacitor, C, through a low-side switch, SL (Figure 5.2). The relationship of input and output voltages is a function of topology and duty cycle, D, which is the ratio of the turn-on time of high-side switch, SH, to switching period. These relationships are derived using the fact that the DC voltage across the inductor is zero in steady state (i.e., inductor zero volt-second principle). For example, in a buck converter, the output voltage, Vo, is equal to the DC value of phase voltage, Vph, and consequently, Vo = DVin. The relationships between key voltages and currents in DC-DC converters are summarized in Table 5.1, and their detailed derivation can be found in most power electronics textbooks [64-66].

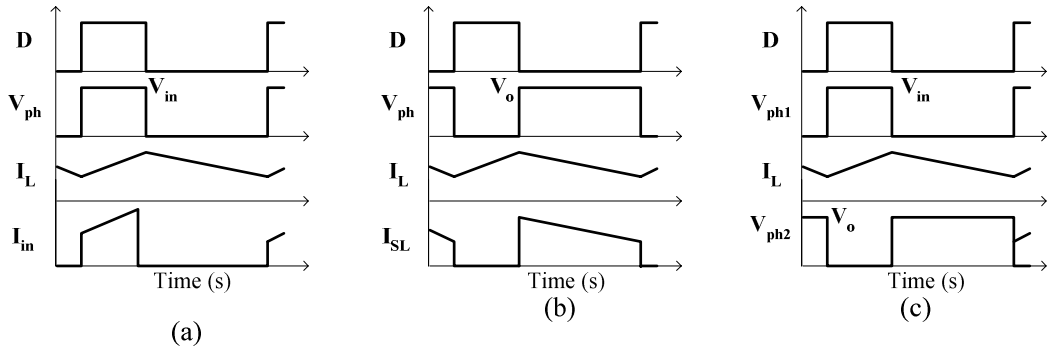


Figure 5.2—Key waveforms of switching regulators in steady state: (a) buck, (b) boost, and (c) buck boost.

Table 5.1—Relationships of key voltages and currents in switching regulators.

Converter	Steady-State Voltage Transfer Function	Steady-State Current Transfer Function	Inductor Current
Buck	$\frac{V_o}{V_{in}} = D$	$\frac{I_{Load}}{I_{in\_AVG}} = \frac{1}{D}$	$I_{L\_AVG} = I_{Load}$
Boost	$\frac{V_o}{V_{in}} = \frac{1}{1-D}$	$\frac{I_{Load}}{I_{in\_AVG}} = 1-D$	$I_{L\_AVG} = \frac{I_{Load}}{1-D}$
Buck-Boost	$\frac{V_o}{V_{in}} = \frac{D}{1-D}$	$\frac{I_{Load}}{I_{in\_AVG}} = \frac{1-D}{D}$	$I_{L\_AVG} = \frac{I_{Load}}{1-D}$

Switches are generally implemented with MOSFETs, bipolar transistors, or diodes [63, 64]. When both S_H and S_L are realized with active switches, the converters are said to be *synchronous* and when one of the switches is realized with diodes, the converters are called *asynchronous*. In synchronous converters, at low load currents, inductor current can go below zero and become reversed, which is not the case for asynchronous converters. When the inductor current does not reverse and clamps to zero, operation is said to be in *discontinuous-conduction mode* (DCM) otherwise it is in *continuous-conduction mode* (CCM) [63, 64].

The conduction loss of low-side switches is higher in asynchronous converters than in synchronous converters because of a higher voltage drop across the diode (i.e., 0.6 V instead of 0.2 V to 0.3 V in the case of an active switch). Nevertheless, there is less switching loss for an asynchronous low-side switch because no driver is needed to turn on and off the diodes. Therefore, synchronous converters achieve higher efficiency than asynchronous converters at high load currents, whereas asynchronous converters reach higher efficiency light loads. Moreover, compensation of regulators in DCM is simpler because of their inherent single-pole frequency response [63, 64], and a converter may be designed deliberately to work in DCM always for ease of compensation.

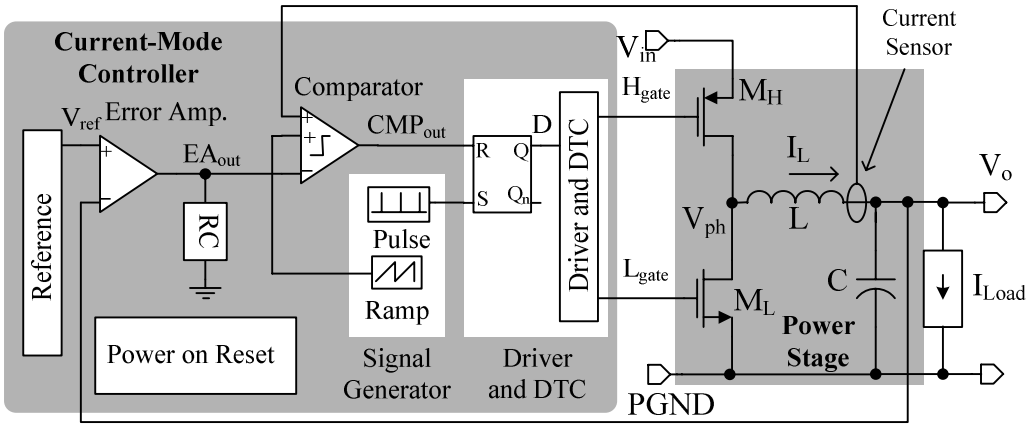
5.2. Controller Schemes

Basic DC-DC converter circuits consist of a few power components. In practice, a feedback loop is applied around the power circuitry to regulate the output voltage and correct the duty cycle in events of load (output current) or line (supply voltage)

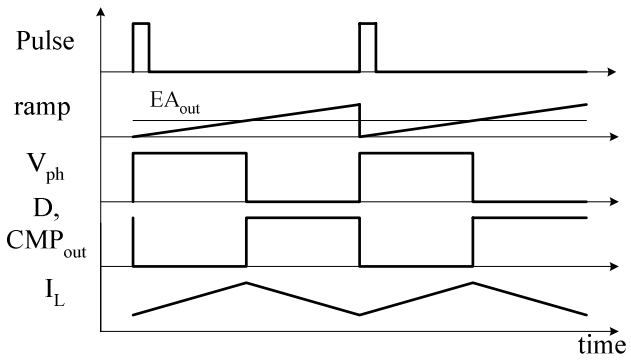
disturbances [63-66]. Many control methods are available and reported for DC-DC converter circuits. These methods can be divided into pulse-width modulation (PWM), pulse-frequency modulation (PFM), and sliding-mode control. Each of the control schemes has subcategories, advantages, and disadvantages [63].

In PWM controllers, the switching frequency is constant, and the duty cycle is modulated to regulate the output voltage. The constant switching frequency of PWM controllers is an important feature when a switching regulator is used in communication systems because the PWM switching noise is well defined and can be attenuated by using filters or carefully choosing switching frequency at system level.

PWM controllers are divided into two main categories: voltage mode and current mode [64]. A simple block diagram of a voltage-mode controller applied to a buck converter is shown in Figure 5.3. High-side switch M_H is turned on and low-side switch M_L is turned off at the beginning of the pulsative signal period through an RS latch. At this point, the error-amplifier output EA_{out} is zero and, therefore, the switching state remains unchanged even when pulsative signal goes to zero. The ramp signal output starts from a minimum at the beginning of a pulse period and goes to a maximum at the end of the period. The error amplifier continuously compares the output voltage to the ramp signal; when the ramp voltage exceeds the output voltage (assuming ramp voltage changes more rapidly than the output voltage), comparator output CMP_{out} becomes positive and resets the RS latch. Thus, in the end, the M_H switch is turned off, the M_L switch is turned on, and inductor current, i_L, reduces.



(a)



(b)

Figure 5.3—Voltage-mode controller: (a) block diagram and (b) corresponding waveforms.

The control loop is not inherently stable (not a single-pole response) in voltage-mode controllers, and its complex double poles should be carefully compensated. Therefore, a voltage regulator compensation network is complex and at least consists of a dominant pole and two zeros to cancel inherent complex double poles. To design a compensator, the inductor L and capacitor C should be known. Therefore, integration of a compensation network for voltage-mode controllers is challenging, if not impossible, for general-purpose converters that use a range of inductor and capacitor values.

Current-mode controllers enjoy several advantages over conventional voltage-mode converters, such as relatively simple compensation requirements because of their inherent single-pole response, cycle-by-cycle current overload protection, and similar transfer functions in both CCM and DCM. On the other hand, current-mode controllers require precise current sensing compared to voltage-mode controllers, where a mediocre current sensing is sufficient over-current protection.

In PFM strategies [63], the switching frequency is not constant because it is used as a control parameter. For example, in constant on-time PFM scheme, the on time of the power switch is constant and a feedback loop modulates the switch off time to regulate the output voltage; therefore the switching frequency is not constant. PFM controllers yield higher power efficiency, especially at low load currents, since their switching frequency decreases at light loads (switching losses are reduces). However, the variable frequency is not appealing in many applications such as telecommunications because of

intermodulation and electro-magnetic interface (EMI) concerns. Furthermore, if switching frequency falls below 10 kHz at low loads, it may cause unpleasant audio noise. As a result, PFM controller operation is typically avoided at frequencies lower than 10 kHz.

Sliding-mode controllers [66] use nonlinear control techniques such as hysteric comparators [63, 66] to achieve the fastest transient response. The output voltage ripple is usually high in sliding-mode controllers and their operation frequency, which depends on parasitic components such as output capacitor ESR is not well defined. Moreover, except for buck converters where simple hysteretic controllers are implemented, the implementation of sliding-mode control is relatively complex, requiring precise on-the-fly current sensing.

Practical control techniques for DC-DC converters are summarized in Table 5.2. The selection of a controller strategy is mainly driven by the application and the specification parameter that is the most difficult to achieve. For example, telecommunication applications are very strict about converter operation frequency; therefore a PWM controller is the choice. However, if the fast transient response is a key specification for a given application, a hysteretic controller may be warranted.

Table 5.2—Summary of control techniques for switching regulators.

Controller	Advantages	Disadvantages
PWM	Constant frequency	Low-efficiency at low loads
Voltage-Mode Controller	No precise current sensing	Complex compensation
Current-Mode Controller	Simple compensation	Precise current sensing
PFM		
Constant On Time	High efficiency at low loads	Variable frequency
Sliding-Mode Controller (Hysteretic)	The fastest available controller	- Not well-defined switching frequency

5.3. Current-Mode Controller

The basic objective of current programming is to transform the power stage into a current source feeding the output capacitance and load and therefore eliminating the inductor effect from frequency response. As a result, the current-programming provides enough damping that the two complex poles of the LC filter split into two real and well-separated poles. The lower pole therefore becomes dominant and produces a

corresponding single-pole response. The operation, compensation, and design of current-mode controllers are discussed next.

5.3.1. Operation

A system-level block diagram of a current-mode controller applied to a buck converter is shown in Figure 5.4 [64]. Instead of the ramp signal in voltage-mode controllers, the error-amplifier output is compared to the inductor current. The RS latch is set at each narrow pulse signal by turning on the high-side switch M_H and low-side switch M_L. As a result, inductor current starts increasing. When the inductor current (converted to voltage at the current-sensing circuit) exceeds the slow-moving error-amplifier output EA_{out} the comparator output CMP_{out} toggles up, resets the RS latch, turns off M_H, and turns on M_L. In steady-state operation, the duty cycle is constant, but under the control of feedback to compensate for the effects of transient events.

A ramp signal is usually subtracted from the error-amplifier output at the input port of the summing comparator to prevent large-signal instability at duty cycles that are more than 50% and reduce noise sensitivity [64, 67, 68]. Intuitively, for a current-mode controller with D more than 0.5, the circuit is converted to a hybrid voltage- and current-mode controller while maintaining the single-pole response of a current-mode controller.

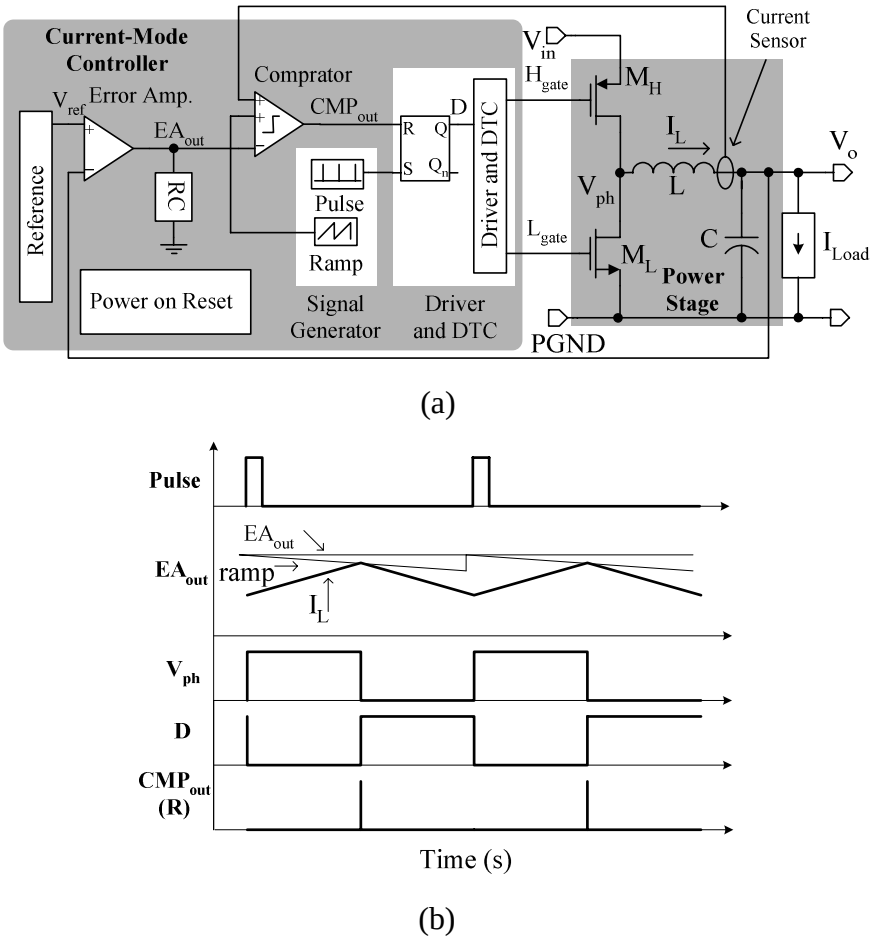


Figure 5.4—Current-mode controller: (a) block diagram and (b) corresponding waveforms.

5.3.2. Compensation

Even though current-mode controllers are inherently stable (i.e., single-pole response), the compensation network is usually added to adjust their voltage-loop DC gain and cross-over frequency. In this section, the key transfer functions of a buck current-mode controller circuit are derived, a practical compensation network is discussed, and the relationship between converter transient and frequency responses is developed.

Small Signal Models

Although a switching regulator is inherently a nonlinear, time-varying system, the simple transfer function concept used to study the stability of linear, time-invariant systems can be used to analyze their stability, if their time-averaged, linearized

approximations are derived [64]. For a switching regulator, the nonlinear section consists of the modulator and switches.

A current-mode controller is a multi-loop feedback system [67, 68]. There are a fast, internal *current loop*, which adjusts the inductor current and a slower, external *voltage loop*, which regulates the output voltage. To analyze the stability of a multi-loop system, every internal loop should be investigated, and all should be stable [67, 68].

The small-signal, low-frequency model of a buck current-mode controller is illustrated in Figure 5.5, where $H_{EA}(s)$ is the transfer function of the error amplifier, $H_L(s)$ is the phase-node-to-inductor current (V_{Ph}-to-i_L) transfer function, and $H_C(s)$ is the transfer function from inductor current to output voltage (i_L-to-V_{out}). $H_L(s)$ and $H_C(s)$ are derived by inspection of Figure 5.6 as

$$H_L(s) = \frac{i_L}{V_{Ph}} = \frac{1 + RCs}{R + Ls + LCRs^2} \tag{5.1}$$

and

$$H_C(s) = \frac{v_o}{i_L} = \frac{R}{1 + RCs}, \tag{5.2}$$

where R is the load AC resistance, C is the value of the output capacitor, and L is the value of the inductor.

In a buck converter, the small-signal transfer function from switch-drive signals to phase node is dV_{in}. Rigorous state-space averaging techniques can be used to derive small-signal switch models for boost and buck-boost converters. The more challenging part is to model the transfer function from input of the summing comparators to switch inputs.

Three different modeling trends, basic [64], Middlebrook [67, 68], and Ridley [69] are noted in literature to analysis current-mode controllers and are discussed next. The basic model only predicts a dominant pole whereas Middlebrook and Ridley are more accurate and predict parasitic poles.

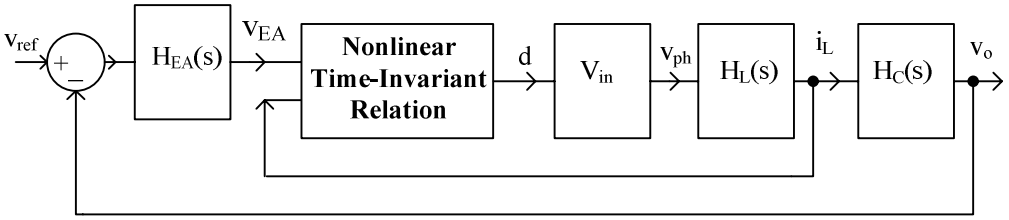


Figure 5.5—Small-signal low-frequency model of current-mode controller.

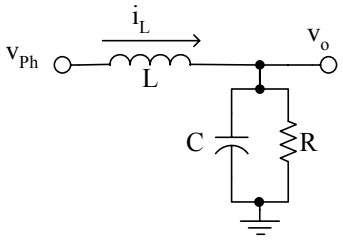


Figure 5.6—Output filter portion of a current-mode controller.

Basic Model

The basic model assumes that the inductor ripple current (ΔI_L) is negligible compared to the average inductor current, and therefore the modulator forces the sensed current to be equal to the error-amplifier output voltage (i.e., $i_L = V_{EA}/R_{Sense}$, where R_{Sense} is the current-sensor gain) [69]. As a result, the current loop, modulator, and inductor are replaced with a current source as illustrated in Figure 5.7. Consequently, assuming no compensation at the error amplifier (i.e., $H_{EA}(s) = 1$), the voltage-loop gain T_v becomes

$$T_v = \frac{v_t}{v_z} = \left(\frac{R}{R_{Sense}}\right)\left(\frac{1}{1+RCs}\right). \qquad (5.3)$$

Equation 5.3 suggests a single-pole response for current programming with a DC gain of R/R_{Sense} and unity-gain frequency ω_{cv} of $1/(R_{Sense}C)$.

The Middlebrook and Ridley models consider the effect of non-zero ripple inductor currents. The Ridley model goes even further and considers second-order effects of output voltage change in an operation cycle, which ultimately transfers the two-loop system to a more complex three-loop scheme [69].

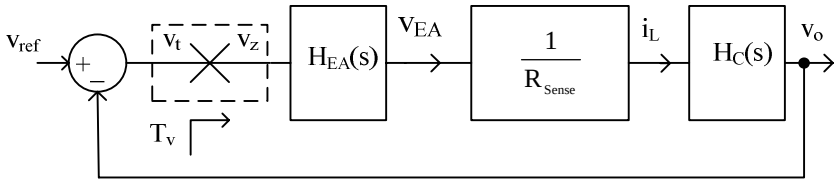


Figure 5.7—Basic small-signal low-frequency model of current-mode controller, assuming negligible ripple inductor current.

Middlebrook Model

The waveforms at the input of the summing amplifier in a current-mode controller are shown in Figure 5.8. The Middlebrook model [67, 68] assumes that the time-averaged value of the inductor current ($<I_L>$) is constant in a switching cycle. At duty-cycle transition X, the instantaneous current, which is the addition of $<I_L>$ and half of the ripple current, is equal to the difference between error-amplifier output and compensation ramp, or equivalently

$$< I_L > + M_1\left(\frac{DT}{2}\right) = \left(\frac{V_{EA}}{R_{Sense}}\right) - M_c DT\,, \qquad (5.4)$$

where $M_1 = (V_{in}-V_o)/L$ is the inductor ramp up slope; $M_2 = V_o/L$ is the ramp down slope; M_c is the compensation ramp slope; V_{in} is the input voltage; V_o is the output voltage; D is duty cycle; and T is switching period. If average inductor current changes by i_L and error-amplifier output changes by v_{EA}, the resultant change in duty cycle is given by

$$d = \frac{1}{(0.5M_1 + M_c)T}\left(\frac{v_{EA}}{R_{Sense}} - i_L\right). \qquad (5.5)$$

Consequently, the summing comparator and RS latch can be replaced with the small-signal modulator model shown in Figure 5.9.

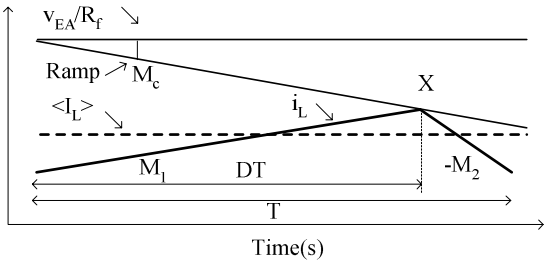


Figure 5.8—Waveforms at the modulator input of a current-mode controller under a steady-state operation conditions: the duty-cycle ratio is determined by the intersection of the inductor current ramp with control voltage plus compensation ramp.

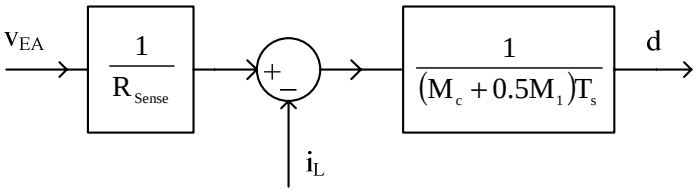


Figure 5.9—Middlebrook's model for the nonlinear time-invariant section of current-mode controller.

Ridley Model

A more accurate way to model current-programming modulators was introduced by Ridley [69]. The Ridley model considers different average inductor currents during the ramping up and ramping down phases of a switching period, as illustrated in Figure 5.10. Thus, the average inductor current in the whole cycle is the weighted average inductor current of the ramp-up and ramp-down phases (i.e., $<I_L>_{DT}$ and $<I_L>_{(1-D)T}$), or equivalently

$$< i_L >_T = D < i_L >_{DT} + (1-D) < i_L >_{(1-D)T}. \qquad (5.6)$$

At the duty-cycle intersection, the inductor average current relates to error-amplifier output, compensation ramp, and ramp-up and ramp-down ripple currents as

$$< i_L >_T = \left(\frac{v_{EA}}{R_{Sense}} \right) - M_c DT - D\left(\frac{M_1 DT}{2} \right) - (1-D)\left(\frac{M_2 (1-D)T}{2} \right). \qquad (5.7)$$

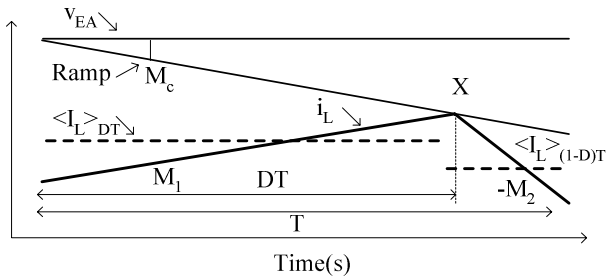


Figure 5.10—Waveform at the modulator input in a current-mode controller assuming a transient operation. The inductor current at the end of a switching cycle is not necessarily equal to the inductor current at the beginning of the same cycle.

If the average inductor current changes by i_L and the error-amplifier output changes by v_{EA}, and considering second-order effects of change in ramp-up and ramp-down slopes, M_1 and M_2, the change in duty cycle d is given by

$$d = \frac{1}{M_c T}\left[\frac{V_{EA}}{R_{Sense}} - i_L - \frac{D^2 T}{2L} v_{in} - \frac{(1-2D)T}{2L} v_o\right], \qquad (5.8)$$

where v_{in} is the small-signal change in input voltage, and v_o is the change in output voltage. Equation. 5.8 is the basis of the Ridley current-mode modulator model whose block diagram is illustrated in Figure 5.11.

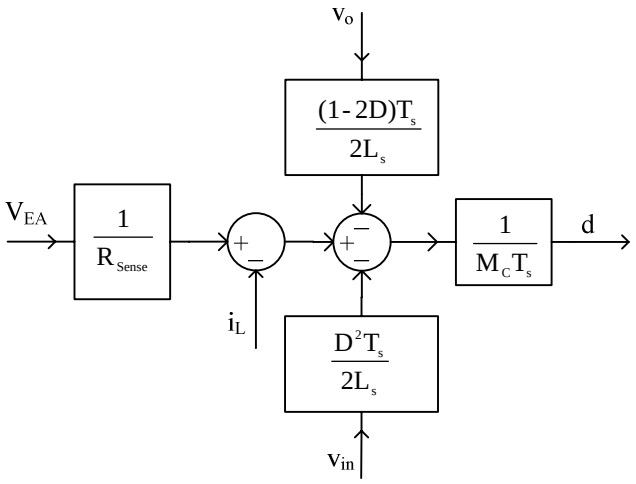


Figure 5.11—Ridley's model for the nonlinear time-invariant section of a current-mode controller.

Current-Loop Stability of Current-Mode Controllers

After the modulator is replaced with a linear, time-invariant model, the dynamics of a current-mode controller can be analyzed with basic control theory, and the stability of current and voltage loops can be verified. Figure 5.12 illustrates a current-mode controller small signal model where the Middlebrook model was replaced for the modulator [67, 68]. To analyze the stability, first the internal current-mode control loop is analyzed by breaking the loop at the output of the current sensor (point 1 in Figure 5.12). The current-loop gain is given by

$$T_i = \frac{i_y}{i_x} = \left(\frac{V_{in}}{(0.5M_1 + M_c)T} \right) \left(\frac{1 + RCs}{R + Ls + LCRs^2} \right). \tag{5.9}$$

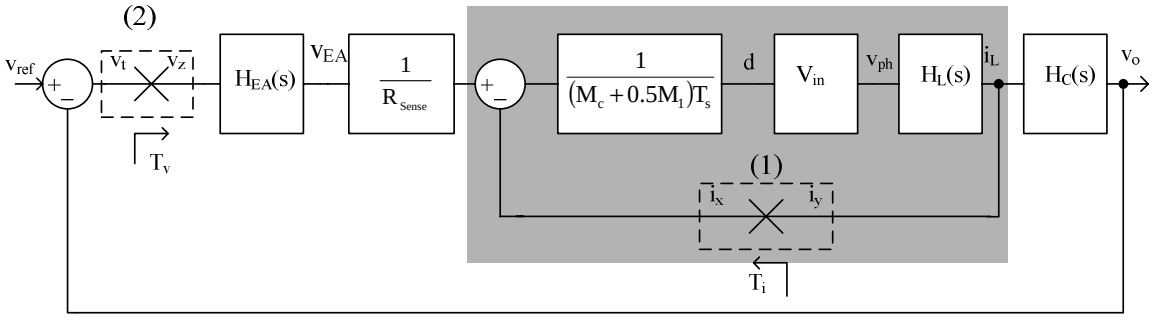


Figure 5.12—Linearized, time-invariant block diagram for a current-mode controller using Middlebrook's model.

The loop gain T_i has a zero at -1/RC and double complex poles at $1/(LC)^{0.5}$. At high frequencies, (R+Ls) << $LCRs^2$ and 1 << RCs and therefore

$$T_i(s \longrightarrow \infty) = \left(\frac{V_{in}}{(0.5M_1 + M_c)T} \right) \left(\frac{1}{Ls} \right). \tag{5.10}$$

Thus, the zero cancels one of the poles, and the current-mode controller effectively provides a single-pole response at high frequencies where its gain drops close to unity. Therefore, the current programming loop is inherently stable (Figure 5.13). The current-mode controller loop unity-gain frequency is given by

$$\omega_i = \frac{V_{in}}{(0.5M_1 + M_c)LT}, \tag{5.11}$$

or equivalently,

$$\omega_i = \left(\frac{1}{1-D}\right)\frac{\omega_s}{\left(0.5(1-D)+\frac{M_c}{M_1}\right)}, \tag{5.12}$$

where ω_s is the switching frequency in radius per second.

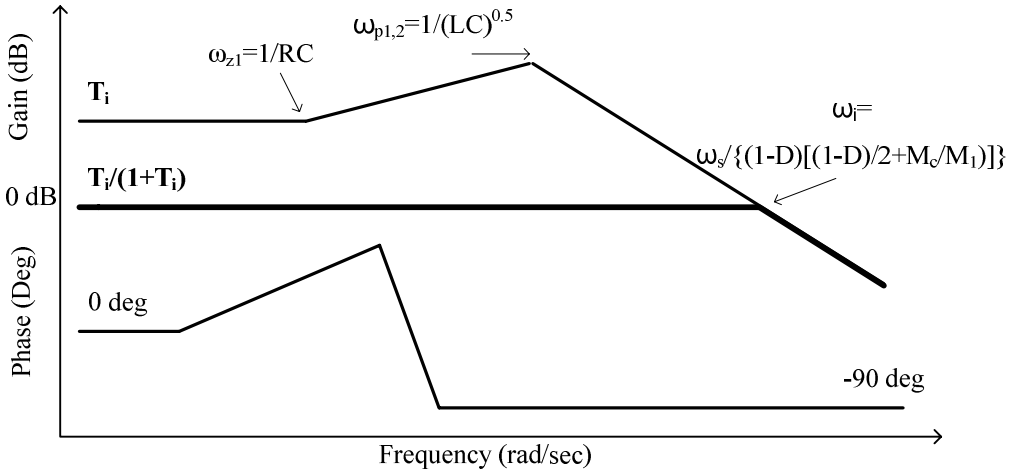


Figure 5.13—Magnitude and phase asymptotes of current loop gain T_i for a current-mode controlled buck converter.

To analyze the external voltage loop, current-programming transfer function is replaced with its closed form, or equivalently

$$\frac{i_L}{v_{EA}} = \frac{1}{R_{Sense}}\left(\frac{T_i}{1+T_i}\right) \approx \frac{1}{R_{Sense}}\left(\frac{1}{1+s/\omega_i}\right). \tag{5.13}$$

As a result, the external voltage loop transfer function is

$$\begin{aligned}\frac{v_o}{v_{EA}} &= \frac{i_L}{v_{EA}}\frac{v_o}{i_L} \\ &= \left(\frac{1}{R_{Sense}}\frac{1}{(1+s/\omega_i)}\right)\left(\frac{R}{1+RCs}\right) \\ &= \frac{R}{R_{Sense}}\frac{1}{(1+RCs)(1+s/\omega_i)}\end{aligned}, \tag{5.14}$$

assuming error-amplifier gain is unity (i.e., $H_{EA}(s) = 1$).

The transfer function without error-amplifier compensation (v_o/v_{EA}) has two poles, a low frequency at -1/RC and a high frequency at the unity-gain frequency of the current loop, ω_i (Figure 5.14). However, since $(1/RC)<<\omega_i$, the crossover frequency of v_o/v_{EA} (ω_c) is at $1/(R_{Sense}C)$, and the loop is stable for the case of a buck converter even without compensation around the error amplifier.

The Middlebrook model predicts the same dominant pole and low-frequency gain as the basic model, but it also shows the reason for the inherent stability of the internal current-mode controller loop and the location of the parasitic pole.

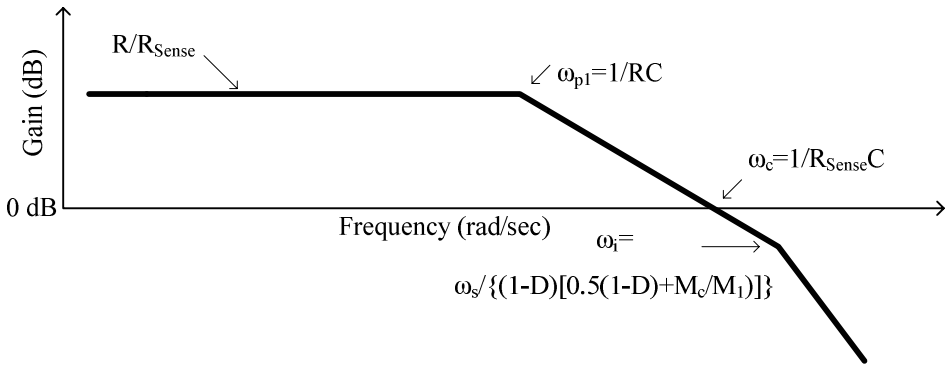


Figure 5.14—Magnitude asymptotes of voltage-loop gain T_v.

Current-Programming Compensation Circuit

Although the current-mode controller is stable without compensation, its voltage-loop DC gain and unity-gain frequency are low, which may result in poor DC accuracy and transient response. The main purpose of adding compensation around the error-amplifier is to increase the gain and cross-over frequency. Although a proportional gain element can be used to increase DC gain and unity-gain frequency at the same time, most of the time an integrator is added to the controller to increase the gain at low frequency, independent of mid-frequency gain that determines the unity-gain bandwidth. One possible approach to implementing the proportional/integrator (PI) controller is shown in Figure 5.15, whose transfer function is given by

$$H_{EA}(s) = \frac{v_{EA}}{v_o} = -\frac{1 + R_a C_{cp} s}{R_b C_{cp} s}, \qquad (5.15)$$

where R_a, R_b, and R_c are resistor values, and C_{cp} is a capacitor value. Figure 5.15 circuit forces a very high gain at low frequency and gain of R_a/R_b at mid frequency when C_{cp} is effectively a short circuit. Resistor R_c sets the DC value of the converter's output. Assuming a high DC gain, the negative input terminal of error amplifier is equal to its positive voltage and hence

$$\frac{V_o}{V_{ref}} = 1 + \frac{R_b}{R_c}. \tag{5.16}$$

The topology given in Figure 5.15 lets the designer program the DC value of V_o by adjusting R_c independent of the AC gain of error-amplifier.

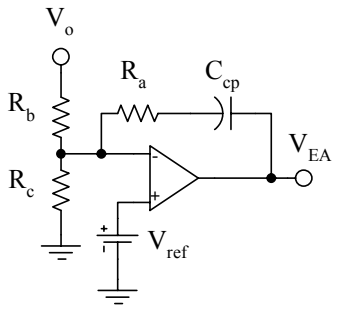


Figure 5.15—Error amplifier and the compensation network around it.

Figure 5.16, shows the loop-gain transfer function for the external loop when the error-amplifier compensation circuit is inserted into the loop. Assuming a high-bandwidth error amplifier, the new crossover frequency occurs at $\omega_{cv} = (R_a/R_b)\omega_c$, where ω_c is the loop crossover frequency without the error-amplifier stage (i.e., $H_{EA}(s)$ is 1). For a stable loop, ω_{cv} should be lower than current-loop pole ω_i, which is close to the switching frequency. A rule of thumb is to limit the external-loop gain bandwidth to less than two-tenths of the switching frequency. Another possible compensation network implementation uses a transconductance amplifier instead of an error amplifier as shown in Figure 5.17.

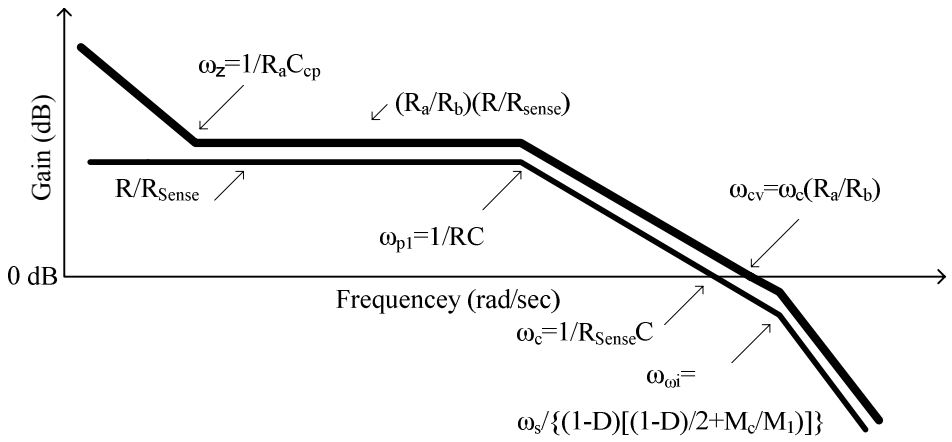


Figure 5.16—Magnitude asymptotes of voltage loop gain, T_v with and without addition of an error-amplifier compensation network.

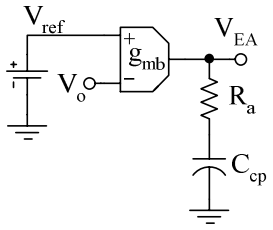


Figure 5.17—An alternative compensation scheme using a transconductance amplifier.

Line and Load Regulation

Line regulation (LNR) and load regulation (LDR) are key figure of merits for voltage regulators irrespective of topology and implementation (i.e., linear, switching, or charge pump). Although regulators are designed to provide fixed voltages at their outputs, they are sensitive to input voltage and load current values because second-order effects. Line and load regulations are defined as

$$\text{LNR} \equiv \frac{V_o\big|_{V_{in}=\max,\, I_{Load1}} - V_o\big|_{V_{in}=\min,\, I_{Load1}}}{V_o} \times 100 \qquad (5.17)$$

and

$$\text{LDR} \equiv \frac{V_o\big|_{I_{Load}=\max,\, V_{in1}} - V_o\big|_{I_{Load}=\min,\, V_{in1}}}{V_o} \times 100\,. \qquad (5.18)$$

These definitions are used mostly in measurements, and the sensitivity of the converter to line and load disturbances can be predicted by output voltage–to-input voltage (v_o/v_{in}) and output voltage-to-load current (v_o/i_{Load}) transfer functions. For the buck current-mode converter, these transfer functions can be derived by inspection of the small-signal block diagram of Figure 5.18 and are given as

$$\begin{aligned}\frac{v_o}{v_{in}} &= D\left(\frac{H_C(s)H_L(s)}{1+T_v}\right)\\ &= \left(\frac{D}{1+A_{DC}}\right)\left(\frac{1}{1+s^2LC}\right)\frac{1}{1+\frac{s}{\omega_{cv}}}\end{aligned} \tag{5.19}$$

and

$$\begin{aligned}\frac{v_o}{i_{Load}} &= \frac{H_2(s)}{1+T_v}\\ &= \left(\frac{R}{1+A_{DC}}\right)\left(\frac{1}{1+sRC}\right)\frac{1}{1+\frac{s}{\omega_{cv}}},\end{aligned} \tag{5.20}$$

where D is the duty cycle; L is the value of the inductor; R is the load AC resistance; C is the output capacitor; T_v is the voltage-loop gain; A_{DC} is the voltage-loop DC gain; and ω_{cv} is the voltage-loop unity-gain frequency. Therefore, to make the output voltage insensitive to line voltage and load current disturbances: (1) the voltage-loop DC gain A_{DC} and (2) the voltage-loop unity gain frequency ω_{cv} should be as high as possible. However, increasing loop DC gain compromises stability, and as will be discussed later, increasing ω_{cv} beyond a critical value has no effect on transient response.

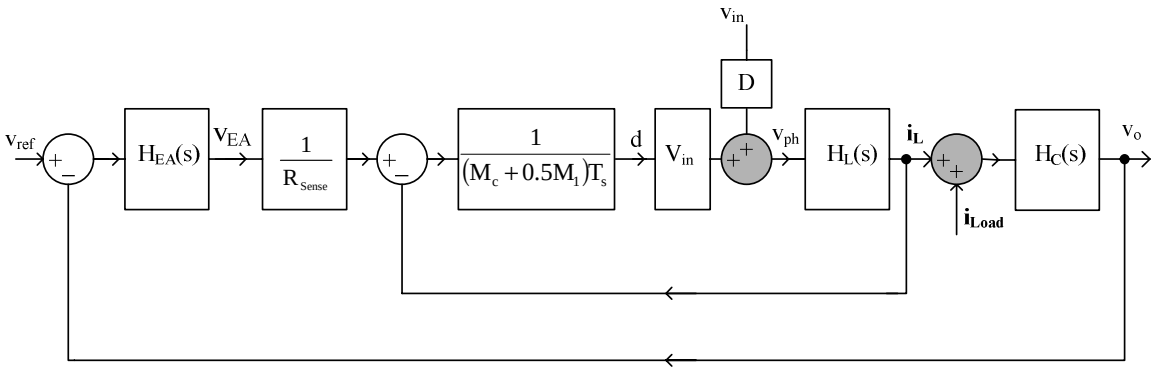


Figure 5.18—Small-signal model block diagram for current-mode controller, including line and load disturbances.

Effect of Error-Amplifier Frequency Response on Loop Stability

The limited bandwidth of the error amplifier creates a parasitic pole in the current-mode controller loop. The parasitic pole degrades the phase margin and may compromise stability. Therefore, the error-amplifier's bandwidth should be high enough to prevent any instability in the converter loop. The error amplifier has a local feedback around it and its effective parasitic pole for the converter loop is given by

$$\omega_{EA} = \frac{GBW_{EA}}{Comp\_Gain}, \tag{5.21}$$

where GBW_{EA} is the error-amplifier gain-bandwidth product, and Comp_Gain is the feedback gain around the error amplifier at mid-band frequencies, where the effect of the low-frequency zero vanishes (i.e., R_a/R_b in Figure 5.15). Considering the effect of the error-amplifier parasitic pole, a rough estimate for the phase margin of the external loop is approximately

$$PM = 180° - 90° - \tan^{-1}\left(\frac{\omega_{cv}}{\omega_i}\right) - \tan^{-1}\left(\frac{\omega_{cv}}{\omega_{EA}}\right), \tag{5.22}$$

where ω_{cv} is the current-mode controller voltage-loop unity-gain frequency and ω_i is the non-dominant pole due to current loop. Therefore, the error-amplifier bandwidth specification can be based on its effect on loop-gain phase margin. For example, to limit the effect of the error amplifier on phase margin to 10°, ω_{EA} should be at least five times

voltage loop unity-gain frequency ω_{cv}. If ω_{cv} = 100 kHz, and a gain of 20 is required around the error amplifier, ω_{EA} should be at least 10 MHz.

Effect of Output Capacitor ESR

Until now, it was assumed that the output capacitor equivalent series resistor (R_{C_ESR}) is low and can be ignored. However, low-cost applications use tantalum capacitors, which have as much as several ohms of ESR, rather than ceramic capacitors with ESRs in the range of milliohms. Relatively high capacitor ESR appears as a zero at $-1/R_{C\_ESR}C$, which can change the dynamics of the control loop.

Stability in Discontinuous Conduction Mode

Asynchronous switching regulators operate in discontinuous-conduction mode (DCM) at light loads. Because of the different operation mechanisms in CCM and DCM modes, their small-signal models are also different. In this mode, output voltage–to-duty cycle (v_o/d) transfer function is a single-pole response, and second-pole and right half-plane zero (in case of boost and buck-boost converters) lie close to the switching frequency, and consequently, much higher than controller voltage-loop gain bandwidth, which is usually designed at 10% to 20% of switching frequency [63]. Because of single-pole response, the operation of switching regulators in DCM mode is inherently stable for most converters.

In a voltage-mode controller, the v_o/d transfer function has two complex poles in CCM and single-pole response in DCM. Thus, the compensation network that stabilizes the regulator in CCM results in stability for DCM operation as well. Employing current-programming results in single-pole response for v_o/d transfer function for both CCM and DCM modes and the loop dynamics are similar in both modes. Intuitively, DCM is inherently a current-programmed controller operation, since it depends on when inductor current reaches zero, which is detected through a rectifier (i.e., diode).

5.3.3. Sub-harmonic Oscillation

A well-known problem with current-mode controllers is their large-signal instability when duty cycle is more than 50%, as illustrated in Figure 5.19 [64]. In steady-state operation, the inductor ripple current is

$$\Delta I_L = M_1 DT = -M_2(1-D)T, \qquad (5.23)$$

where D is the duty cycle; T is the switching period; and M_1 and M_2 are inductor ramp-up and ramp-down slopes, respectively. If a disturbance $i_L(0)$ changes the sensed inductor current at the beginning of a switching cycle, the change in duty cycle D is

$$i_L(0) = M_1 dT . \tag{5.24}$$

As a result, the inductor current error from the initial disturbance at the end of the switching period becomes

$$i_L(T) = M_2 dT = \frac{M_2}{M_1} i_L(0) . \tag{5.25}$$

If the relationship of M_1 and M_2 with input and output voltages are considered, the relationship between current disturbance at the end and beginning of the switching cycle becomes

$$\frac{i_L(T)}{i_L(0)} = -\frac{D}{1-D} . \tag{5.26}$$

As a result, for D more than 50%, disturbances tend to grow cycle by cycle, which results in large signal instability. Ultimately, the feedback loop tries to regulate the output voltage, which results in stable inductor waveforms that repeat themselves at one-half, one-third, or one-fourth of the switching frequency, which is how the sub-harmonic oscillations originate. Operation in sub-harmonic oscillation mode is undesirable because of its adverse effect on efficiency since inductor ripple current is increased and so do its associated power conduction losses.

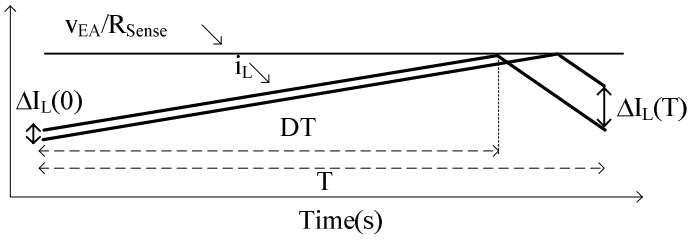


Figure 5.19—Effect of initial perturbation on inductor current.

To avoid sub-harmonic oscillations and reduce the sensitivity of the current-programming to noise at the output of the current sensor, a compensation ramp is added

to the output of the error amplifier, as illustrated in Figure 5.20. The relationship between duty cycle D current ramp-up and -down slopes M_1 and M_2, compensation ramp M_c, period T, and inductor ripple current is

$$M_1 DT + M_c DT = \Delta I_L \tag{5.27}$$

and

$$M_2 (1 - D)T + M_c DT = \Delta I_L . \tag{5.28}$$

If a disturbance $i_L(0)$ changes the sensed inductor current at the beginning of a switching cycle, the change in duty cycle d is

$$i_L (0) = d(M_1 + M_c)T . \tag{5.29}$$

Consequently, the inductor current error from the initial disturbance at the end of the switching period becomes

$$i_L (T) = d(-M_2 + M_c)T , \tag{5.30}$$

or equivalently,

$$i_L (T) = -\left(\frac{M_2 - M_c}{M_1 + M_c} \right) i_L (0) = -K_G i_L (0) . \tag{5.31}$$

With a proper selection of the compensation ramp slope M_c the growth factor (i.e., K_G) can be limited to less than one, preventing large-signal stability in the process. Rearranging the growth factor, the following design equation is structured:

$$\left(\frac{D}{1 - D} \right) < \left(1 + 2\frac{M_c}{M_1} \right). \tag{5.32}$$

Therefore, a lower limit for M_c exists to prevent sub-harmonic oscillations for the maximum duty cycle, given maximum duty cycle conditions. Intuitively, adding a compensation ramp results in a hybrid of current- and voltage- mode controllers.

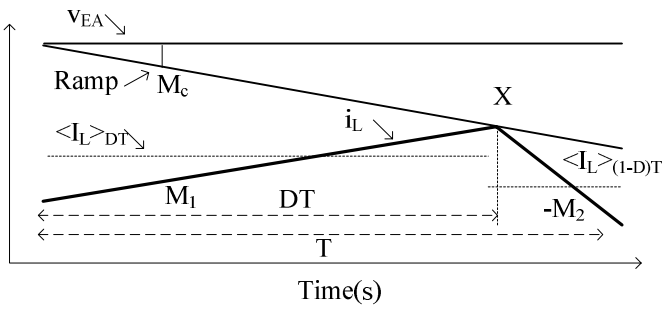


Figure 5.20—Steady-state and perturbed waveforms in the presence of an artificial ramp.

Summing Comparator Delay

The summing comparator compares the output of the error amplifier with the sensed current. When the sensed current exceeds the error amplifier output, the comparator output becomes high and resets the SR latch. The most important characteristic of the comparator to be specified is its propagation delay. If the comparator delay is short, the output of the comparator (R signal) has short pulse width. As the comparator delay increases, the reset signal (R) remains high and its pulse width increases. For proper operation, the reset signal should become low before the rest of the next set signal from the pulse generator. System-level simulations show that if comparator delay exceeds a critical value, the loop operation goes into sub-harmonic operation because the reset signal remains high when a new pulse signal arrives causing the RS latch to go into an illegal state, which then results in skipping a set pulses every other period. Consequently, top-level simulations should be performed to determine the acceptable upper limit for the summing comparator delay. A rule of thumb is for a comparator propagation delay to be on the order of 5% of the switching frequency with overdrive voltages around 10 mV.

5.3.4. Transient Response

The higher the closed-loop gain bandwidth is in a system, the faster it responds to disturbances and transient events such as line and load dumps. This subsection discusses the relationship between the converter's loop bandwidth and its transient response, and derives a critical bandwidth above which increasing a regulator's bandwidth does not improve transient response [70, 71].

The relationship between the gain bandwidth and transient response time is well known in single-pole, linear, and time-invariant systems. For these systems, the transfer function from input to output is

$$\frac{V_o}{V_{in}} = \frac{A}{1+\frac{s}{\omega_{3dB}}}, \tag{5.33}$$

where A is the DC gain and ω_{3dB} is the 3 dB bandwidth. For this system, the transient response to a step input $V_{in}u(t)$ is $V_o = AV_{in}(1-e^{-t/\omega_{3dB}})$, whose 10% to 90% rise time is given by $t_r = 2.2/\omega_c$.

The objective of this section is to determine how the converter responds to a load transient. The worst-case load transient occurs when the load current changes abruptly (in a few nanoseconds) from its minimum to its maximum or vice versa. The controller cannot respond to the load transition in few nanoseconds, since its bandwidth is limited to few hundred kilohertz. Before the loop can respond to a fast load transient by changing inductor current, output capacitor C provides the entire load current. Therefore the output voltage changes because of the capacitor and its ESR. The loop then slowly compensates for the changes in output voltage by altering the inductor current. In most of today's applications, the output voltage should not change more than a few tens of millivolts while responding to worst-case load transients. The value of output capacitor C is usually selected around a few tens of microfarads, but the use of extremely large capacitors is avoided because of their cost and space consumption. Moreover, large capacitors are avoided when the output voltage is not constant, and the output voltage should be programmed to a new value within a few microseconds in applications such as micro-processors and adaptive supplies for RF power amplifiers.

Yao et al. discussed the relationship of loop bandwidth and transient response for PWM voltage- and current-mode controllers [70, 71]. Here, only their analysis of current-mode control transient response is presented. A diagram of current-mode control including a transient load I_{load} is shown in Figure 5.21. Transfer function, $H_C(s)$, is

$$H_C(s) = \frac{1}{sC} + R_{C\_ESR}, \tag{5.34}$$

where capacitor ESR R_{C_ESR} is included and an ideal load ($R \to \infty$) is assumed. From Figure 5.22, the inductor current response to a transient load is

$$\frac{i_L}{i_{Load}} = \frac{T_v}{1+T_v}, \tag{5.35}$$

where T_v is the voltage loop gain. Assuming a relatively high DC loop gain, the previous relation simplifies to

$$\frac{i_L}{i_{Load}} \approx \frac{1}{1+\frac{s}{\omega_{cv}}}, \tag{5.36}$$

where ω_{cv} is the voltage loop unity-gain frequency. Therefore, the response of inductor current to a transient load step $I_{Load}u(t)$ becomes

$$i_L = i_{Load}(1-e^{-t/\omega_{cv}}). \tag{5.37}$$

Consequently, the output voltage ripple after a transient load dump is given by

$$v_o = \frac{1}{C}\int i_c\,dt + R_{C\_ESR} i_c, \tag{5.38}$$

where i_c is the capacitor current, which is the difference between inductor current and load current. After simplifying the previous two equations, the output voltage ripple from the transient load becomes

$$v_o = i_{Load}\left[\frac{1}{C\omega_{cv}}(e^{-t/\omega_{cv}} - 1) - R_{C\_ESR}e^{-t/\omega_{cv}}\right]. \tag{5.39}$$

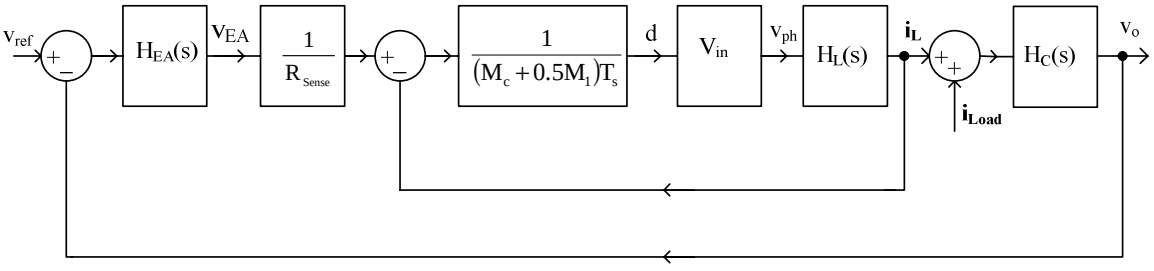


Figure 5.21—Small-signal model used to predict the effect of a load dump on inductor current.

Investigation of the previous relationship shows that there is a critical bandwidth that minimizes the output ripple, which is determined by differentiating the previous equation with respect to ω_c and equating it to zero. Therefore, critical bandwidth is

$$\omega_{ct} = \frac{1}{R_{C\_ESR}C}. \tag{5.40}$$

Consequently, the maximum output voltage ripple resulting from a load dump I_{Load} is

$$v_{o(max)} = \begin{cases} \dfrac{I_{Load}}{C\omega_{cv}} & \omega_{cv} < \omega_{ct} \\ R_{ESR\_C}I_{Load} & \omega_{cv} > \omega_{ct} \end{cases}. \tag{5.41}$$

These equations show that there is a critical bandwidth value beyond which increasing bandwidth does not reduce the voltage ripple ass shown in Figure 5.22 (a). At a transient load event, all of the transient load current is supplied from the capacitor at first and therefore output voltage changes by $R_{ESR\_C}I_{Load}$. If the regulator bandwidth is high enough, the regulator starts to compensate for the output voltage change immediately but it cannot compensate for the instantaneous drop of capacitor ESR (Figure 5.22(b)). On the other hand, if the regulator bandwidth is low, there is a delay before controller starts to compensate for the change and therefore output voltage transient ripple becomes larger (Figure 5.22 (c)).

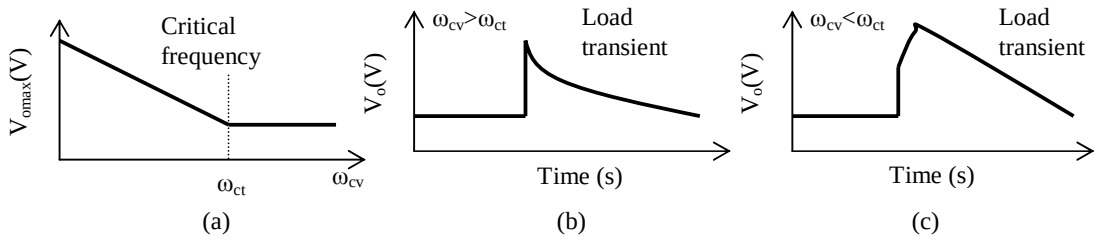


Figure 5.22—Output voltage drop from a load dump: (a) output voltage versus frequency, (b) transient response for $\omega_{cv}>\omega_{ct}$ and (c) transient response for $\omega_{cv}<\omega_{ct}$.

The foregoing calculation for the relationship of transient response and controller bandwidth is valid only if the controller is not saturated. Limited by the topology of the

switching regulators, inductor current in a buck converter can rise and fall only as fast as $di_L/dt = (V_{in} - V_o)/L$ and $di_L/dt = -V_o/L$, respectively. The maximum rate of change of the inductor current in the voltage loop (Eq. 5.37) is $di_L/dt = I_{load}/\omega_{cv}$. Therefore, to guarantee an "unsaturated" transient response (i.e., inductor current rise and fall time controlled by linear loop rather than natural rise and fall slopes), the inductor value should be less than the critical value given by

$$L < \left(\frac{V_{in}}{I_{load}\omega_{cv}} \right) \mathrm{Min}(D, 1-D) = L_{ct}, \qquad (5.42)$$

where D is the duty cycle and ω_{cv} is the controller voltage-loop unity-gain frequency. More detailed explanation can be found at the references [70, 71].

5.4. Controller Design

There are often several solutions to a design problem. In a design problem with several design variables, a few solutions exist that satisfy the specifications [64-66, 72]. Usually, designers optimize the solution for one or several key parameters, while closely meeting other non-critical parameters. As a first step in the design process, a circuit topology should be chosen that best satisfies the more challenging specification parameters. After the topology is chosen, the design parameters whose values affect only a single specification parameter are determined, and then trial and error is used to find solutions for parameters whose values affect several specification parameters. The following strategy is presented as a method for designing current-mode controllers, but the steps can be generalized to any controller topology once the proper design equations are replaced. The strategy is applied to the design a buck converter for a handheld micro-processor application, whose specifications are given in Table 5.3.

Table 5.3—Specifications for a buck converter used in a Li-Ion battery-supplied handheld micro-processor application.

Specification Parameter	Value
Input Voltage	2.7 V to 4.2 V
Output Voltage	1.5 V
Load Current	<1 A
Ripple Current	0.2 A
Switching Frequency	1 MHz
Output Voltage Ripple	± 5% (± 75 mV)
Efficiency η	>80%

The design steps are as follows:

1. The switching frequency f (i.e., period T) is set from the specification list for low value of capacitor and inductor to 1 MHz.
2. The ripple current (ΔI_L) is selected to be 20% of maximum current load ($\Delta I_L \approx$ 0.2A) as a compromise between high efficiency, which requires low current limit, and high transient response, which needs high ripple values.
3. The duty cycle is calculated from input and output voltages (D = 0.35 to 0.56).
4. The inductor is selected by using $V = L\frac{\Delta I}{\Delta t}$ and $V_{in} - V_o = L\frac{\Delta I}{DT}$ considering $L < \left(\frac{V_{in}}{I_{load}\omega_c}\right)\text{Min}(D, 1-D) = L_{ct}$
5. The compensation ramp slope is designed from $\frac{D}{1-D} < 1 + \frac{2M_c}{M_1}$ to prevent sub-harmonic oscillation if the duty cycle exceeds 50%. Thus, M_c=0.1 V/μsec.
6. The current-sensing gain (R_{Sense}) is selected for a suitable voltage range at maximum inductor current (e.g., for 1 A inductor current, a voltage range of 0.5 V was chosen, R_{Sense} = 0.5 Ω).
7. The ramp signal peak-to-peak voltage (V_p) is selected from $M_c = V_p/(R_{Sense}T)$. Thus, V_p=0.1 V.
8. Output voltage accuracy (DC + transient) specification (ΔV_{omax}) is divided into maximum allowable ripple for DC and transient situations. Since satisfying transient ripples is more challenging, $0.25\Delta V_{omax}$ is dedicated for DC and

$0.75\Delta V_{omax}$ is dedicated to transient ripple. Thus for ΔV_{omax} =±75 mV, the controller is designed for approximately ±18 mV steady-state and ±56 mV transient ripple.

9. The output capacitor C is chosen to limit the steady-state output voltage ripple to $0.25\Delta V_{omax}$ by using $V_{rp} = \Delta I/(8C)$. Thus C>0.7 μF. Therefore, safely a 47 μF capacitor was selected.
10. The voltage-loop gain and unit gain frequency is calculated without compensation.
11. The current-loop parasitic pole is calculated from $\omega_i = \frac{1}{1-D}\frac{\omega_s}{[(1-D)/2 + M_c/M_1)]}$
12. The critical bandwidth is calculated in current-mode controller, by $\omega_{ct\_i} = \frac{1}{R_{C\_ESR}C}$. For example, for the given application and assuming 10 mΩ capacitor ESR, f_{ct_i}=338 kHz.
13. For fast transient response to load or line disturbances, the voltage-loop unity gain frequency ω_{cv} is selected to be as high as possible. However, the following facts should be considered:
    a. For a stable operation without complex compensation, $\omega_{cv} < \omega_i$.
    b. There is no benefit in increasing ω_{cv} beyond critical frequency $\omega_{ct.}$.
    c. To prevent a saturated response, $L < \frac{V_{in}}{I_{load}\omega_{cv}}\min(D,1-D) = L_{ct}$.
14. Transient output voltage ripple is predicted by $v_{o(max)} = \begin{cases} \frac{I_{load}}{C\omega_c} & \omega_{cv} < \omega_{ct} \\ R_{C\_ESR}I_{load} & \omega_{cv} > \omega_{ct} \end{cases}$
15. Redesigns of inductor, voltage loop unity gain frequency (ω_{cv}), and output capacitor are repeated until all specifications are satisfied.
16. The value of resistors. R_a and R_b, in the compensation network are determined for the selected voltage-loop unity gain frequency ω_{cv}.

17. Low-frequency gain can be increased for optimum DC regulation without affecting high-frequency response through addition of a low-frequency pole-zero pair.
18. Power MOSFET switch sizes are selected to satisfy efficiency specifications.

The designed parameters of a current mode controller to satisfy the specification in Table 5.3 are summarized in Table 5.4.

Table 5.4 List of design parameters to satisfy specification of Table 5.3.

Design Parameter	Value
L	3.9 μH
C	47 μF
R_a	15 kΩ
R_b	1 kΩ
R_c	2 kΩ
C_{cz}	20 nF
R_{Sense}	0.5 V/A
Compensation Ramp Slope	0.1 A/μs
Voltage-Loop Bandwidth	100 kHz
M_H R_{on}	50 mΩ
M_L R_{on}	50 mΩ
Error Amplifier GBW	10 MHz
Summing Comparator Delay	<70 ns for 10 mV overdrive

SUMMARY

The operation of DC-DC converters was reviewed in this chapter and challenges in the design of current-mode controller systems were discussed. First, the dynamics of a current-programming loop was studied and the location of dominant and parasitic poles from internal current loop and error-amplifier bandwidth were determined. Then, a critical upper limit bandwidth was derived, above which, increasing the current-programming bandwidth does not improve the transient response. The results of the discussion were used to design a current-mode controlled buck converter suitable for portable Li-Ion applications. The requirement of the current-mode controller for precise current sensing is used to set it up as a test bed to verify the precision of the proposed current sensor. Circuit implementation of the proposed current sensor and current-mode controller is presented in the next chapter.

CHAPTER 6

CIRCUIT DESIGN

Thus far, a self-calibrating, lossless, and accurate current-sensing technique for switching regulators was proposed in Chapter 3; its sub-block specifications were derived in Chapter 4; and a current-mode-controlled PWM was designed as its test bed in Chapter 5. This chapter discusses the circuit design of a fully integrated prototype of the proposed technique and its test bed, current-mode controller, in 0.5-µm CMOS process. Although design of each circuit block is discussed, more emphasis is given to the design of a few high-performance blocks, including a low-offset, low-glitch, highly linear, adjustable gain and bandwidth g_m-C filter; a tuning circuit; an ultra low-offset calibration circuit; and low-power wave generator. The experimental results for the performance of each individual block are also provided, but the system-level results are presented and discussed in the next chapter.

6.1. System

The basic block diagram of the proposed current-sensing technique and its current-mode controller test bed is depicted in Figure 6.1. The power stage, which includes power switches M_H and M_L, the inductor L, and capacitor C, is off chip. The proposed chip includes the proposed current-sensor and current-mode controller blocks. The objective of the proposed technique is to implement an integrated current sensor to measure inductor current in a lossless, precise, and accurate manner. The current-sensor core is an on-chip, first-order low-pass g_m-C filter with adjustable gain and bandwidth. This circuit measures inductor current losslessly since it only processes inductor port voltages, and no extra sense element is placed in the inductor current path. The technique is accurate if the on-chip filter is matched to inductor characteristics [1] (i.e., $RC = L/R_{ESR}$ and $(g_mR)R_{ESR} = \alpha$, where R, C, and g_m are filter resistor, capacitor, and transconductance, and L and R_{ESR} are inductor inductance and ESR, respectively). Therefore, tuning and calibration blocks are added to adjust the filter to the inductor at the startup, when the chip is just powered up and before the converter starts regulating the

output voltage. A test current, I_{TEST}, is forced into the inductor during tuning and calibration, when both power switches M_H and M_L are turned off. This current is a triangular wave at tuning and a constant DC at calibration.

To eliminate the sensitivity of the tuning and calibration loops to the parasitic resistances and inductances of inductor-to-filter and inductor-to-current generator connections, a four-wire sensing scheme was used. Unlike inductor L and capacitor C, power switches can be integrated in today's technology. However, these FETs require large die areas and access to state-of-the-art packages, assembly, and bond wires to reduce switch "on" resistance to few milliohms. Due to resource limitations for manufacturing, it was decided to implement these switches with discrete elements.

AMI's 0.5-μm CMOS process was chosen from other available processes (i.e. AMI's 1.5-μm and TSMC's 0.5-μm), because of its high-value poly-resistors (1 kΩ/□) and poly-poly-capacitors (1 fF/□), where there is a large demand for them in power-management circuits. Moreover, there are 10 fabrication runs each year for AMI's 0.5-μm CMOS process through MOSIS, which facilitates scheduling of tape-outs.

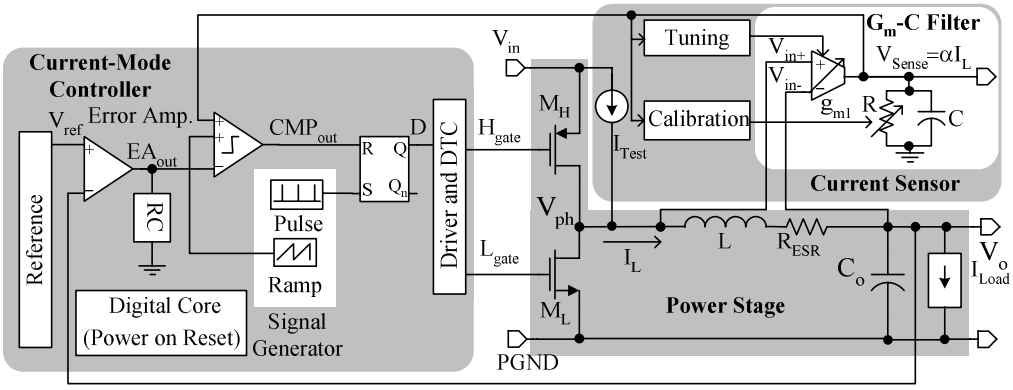


Figure 6.1—Basic top-level block diagram of the proposed chip.

6.1.1. Hierarchy

Divide-and-conquer is a well-known approach to addressing complex problems, which separates the problem to several blocks with lower complexity. Using this general guideline, the proposed system was divided to five manageable sub-systems: current-

sensing block, current-mode controller, wave generator, digital core, and reference and biasing block.

The current-sensing block includes the building blocks of the proposed current-sensing technique: a programmable, low-offset g_m-C filter, a tuning loop, and a calibration circuit. The g_m-C filter itself is a complex circuit, and it has its own hierarchy to facilitate its design. The current-sensing block also includes a test–current generator that converts the voltage signals from the wave generator and reference circuit to currents, and forces these test currents into the inductor at startup. A clock generator that provides auto-zeroing clocks for the g_m-C filter, tuning, and calibration loops is another part of the current-sensing block. The last circuit in this category is a simple inverting buffer that is necessary to interface g_m-C filter output with the current-mode controller sensed-current input (i.e., the input of the summing comparator).

The current-mode controller is another complex top-level block, and it consists of an error amplifier, summing comparator, driver and dead-time control (DTC), and soft-start sub-blocks. The third main top-level block is the wave generator that is responsible for providing triangular, ramp, and pulse signals for the tuning and calibration circuits and for the current-mode controller. The reference and biasing circuit is a housekeeping block that provides voltage reference and bias currents for all other circuits on the chip. The digital core is the system brain, in a way, and controls the interaction between blocks during startup (i.e., tuning, calibration, and normal operation). The first two levels of the proposed chip hierarchy are summarized in Table 6.1.

Table 6.1— Hierarchy of the final chip.

Hierarchy Level 0	**Hierarchy Level 1**	**Hierarchy Level 2**
Proposed Chip Top Level	Current-Sensing Block	G_m-C Filter Tuning Loop Calibration Loop Clock Generator Inverter Amplifier Test Current-Generator VGND Buffer
	Current-Mode Controller	Error Amplifier Summing Comparator Driver and Dead-Time Control (DTC) Soft Start-up
	Wave Generator	Triangular/Ramp/Pulse Generator
	Digital Core	Digital Core
	Reference and Biasing	Reference and Biasing

6.1.2. Floorplanning

The physical layout of high-performance analog and mixed-signal integrated circuits is as important as their design. Parasitic capacitance, resistance, and inductance in signal paths as well as coupling from switching nodes to sensitive high-impedance nodes are practical layout issues that cause integrated circuits to underperform or even fail.

For best results, floorplanning, which is planning how different blocks of a system are placed relative to each other on the die, should be performed in the early stages of the design and before layout starts. At this stage, the layout area of each block in the circuit is estimated, pin dedications for critical inputs and outputs are completed, and the block positions in the top-level layout are determined. Usually circuits, inputs and outputs, and internal signals are partitioned to sensitive analog (e.g., bandgap), insensitive and low noise digital (e.g., digital core and enable/disable signals), and noisy high-frequency digital (e.g., switching node and clock generator) blocks. The floorplanning, pin dedications, and routing should be arranged to minimize the interaction between sensitive and noisy blocks and routes. The noisy and sensitive blocks should be put as far as possible from each other and guard rings should be used for further isolation. Figure 6.2 shows the initial floorplanning of the proposed chip. Although the rectangular shape of the chip is selected to fit in the minimum number of MOSIS tiny chips, a square die shape is a better choice since it results in best yield for the same area.

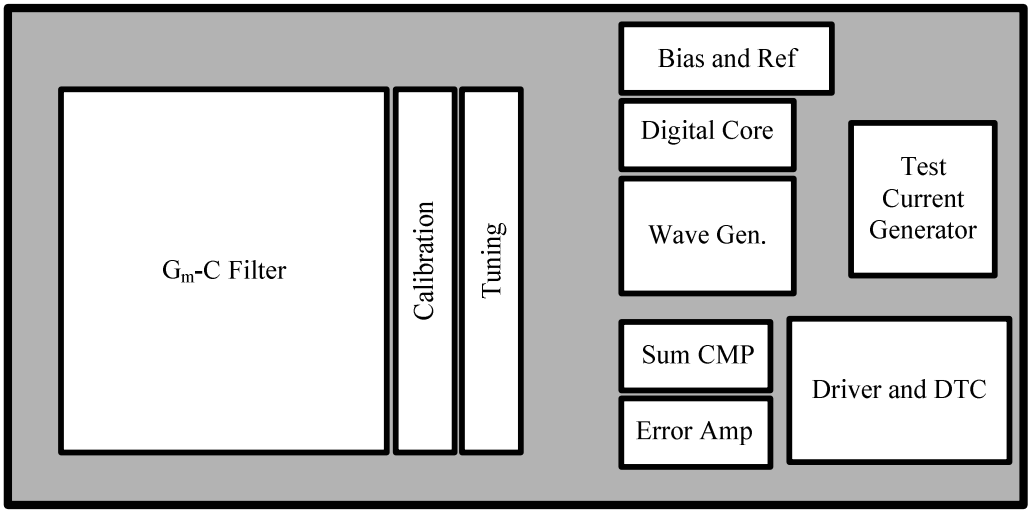


Figure 6.2—Initial floorplanning of the final chip.

At the early stages of the design, it was decided to use separate analog, digital, and power ground routes and pins to achieve high accuracy. Ground is a node in the circuit where other voltages are referenced to it. The parasitic resistance and inductance of the metal routes and non-zero currents cause voltage drop among the nodes that are supposed to be at the same potential. Although a large metal area can be dedicated on the PCB to reduce these parasitic elements and increase the ground quality, the same trick cannot be used on a chip because of area limitations and the relatively high value of resistance and inductance of on-chip metal layers and bond wires. To address this issue, most power management designers separate the analog, digital, and power grounds on the chip, bring them off-chip through different bond wires, and connect them using the star method on the PCB, where parasitic elements are minimal (See Appendix B for details).

Design of electrostatic discharge structures (ESDs), which are part of any practical circuit, are also handled in the floorplanning stage. Design of ESDs is usually empirical and they are usually provided by the IC-fabrication facility for each process. Nevertheless, these structures were not implemented in the prototype IC and were removed from the MOSIS standard pin frame because of area limitations and to fit the design in two MOSIS tiny chip areas.

6.1.3. Design Flow

Circuit design flow for the proposed chip started from system-level specification for the proposed current-sensing technique and current-mode controllers, establishing specifications for sub-blocks as they were discussed in Chapters 3, 4, and 5. A simple top-level architecture was then set up and simulated using simple behaviorally-based macro-models, after which specifications for each block were verified. After the system-design phase was finished, transistor-level design of individual blocks was performed. Then, each designed block was simulated and verified against its specific target specifications, both nominally and over process corners and temperature extremes using Cadence™ corners and Monte-Carlo tools. Before having the design fabricated (i.e., before *tape-out*), all the sub-blocks were interconnected and simulated together, which constituted the transistor-based, top-level system. For a systematic approach, a top-down design strategy was applied when possible. Priority was given first to designing the high-

performance challenging blocks, such as g_m-C filter, tuning loop, and calibration circuit, which were key to verifying the proposed current-sensing technique,.

The nature of integrated circuits makes their debugging and characterization very hard, if not impossible, without a design for test strategy at design time. Keeping this in mind, the proposed chip blocks were designed to include test modes to bring out internal critical signals, disable key functional blocks, and replace them with external circuits to achieve full test coverage and the ability to test the system even when a block critical to system operation, but not critical to verification of the proposed current-sensing concept, (e.g., voltage reference) fails. Additionally, pads were added on the critical nodes that were not connected to the pins to probe them if necessary. Design rule check (DRC) and layout-versus-schematic (LVS) verifications were also performed before the tape-out to validate the physical design.

6.2. Circuit Blocks

Design of circuits for the integrated prototype is discussed in the following 14 subsections. For each circuit, the schematic, design parameters, worst-case simulations, and nominal test results are provided. More emphasis is given to complex circuits, such as the g_m-C filter, tuning loop, calibration circuit, and wave generator, where the circuit contributions of this thesis reside.

6.2.1. G_m-C Filter

Low-offset operation of filters can be as important as their high-frequency response, as is the case for measurement and instrumentation applications, where the DC portion of the signal contains important information. When sub-millivolt input-referred offsets are required, such as in sensor applications, increasing the dimensions of critically matched CMOS transistors is not practical, and dynamic offset-cancellation circuit techniques are therefore necessary. Additionally, if the circuit is analog and continuous, low-offset operation must also remain continuous, negating the attributes of simple auto-zeroing schemes. Although the appearance of spikes and glitches is inherent in dynamic offset-cancellation circuits because of their switching nature, glitches of more than a few millivolts cannot be tolerated in some high-performance applications because of noise sensitivity. For example, if undesirable glitches appear at the input of a high-speed, high-

resolution comparator, they trigger unwanted transitions, which adversely affect system performance parameters like noise and jitter. Tuning the gain and bandwidth of analog filters is also increasingly important in a wide range of applications, such as radio-frequency (RF) filters in receivers, where the filter bandwidth must match the received signal frequency to discern the signal from the noise present.

The filter needed for the proposed current-sensing technique should be low-offset for high precision since its input at normal operation and especially during start-up are relatively small. Moreover, the low-offset operation should be continuous and low-glitch since inductor current information is continuously monitored in controller loop. The basic filter circuit consists of a programmable transconductance g_m, an adjustable resistor R, and a capacitor C (Figure 6.3). However, the basic topology cannot satisfy the sub millivolt input-referred offset requirement forced by low value of dc voltage across the inductor, and therefore dynamic offset-cancellation circuits are needed. Programming the gain and bandwidth of the filter is necessary for accuracy to adjust the filter bandwidth to inductor cutoff frequency [73]. While the filter bandwidth is only a few kilo-Hertz, its single pole response extends through several decades of frequency and parasitic poles must therefore lie well above the operating frequencies of the system, which can easily exceed 10 MHz. Rail-to-rail input common-mode range (ICMR) at positive input and high linearity are also required to prevent distortion at the output. Currently, state-of-the-art solutions for current-sensing filters in DC-DC converter applications are discrete, where the filter gain and bandwidth are adjusted manually through off-chip resistors and capacitors [73].

The rest of this section is organized as follows: First, dynamic offset-cancellation techniques are reviewed and ping-pong auto-zeroing is chosen to achieve continuous low-offset operation; then, the proposed continuous low-offset, programmable gain and bandwidth filter is introduced and detailed circuit implementation of the filter is discussed. Finally, experimental results are presented and conclusions are drawn.

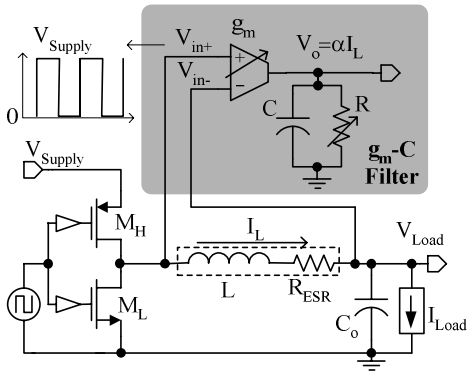


Figure 6.3— Programmable gain and bandwidth g_m-C current-sensing filter applied to a buck switching.

Review of Offset-Cancellation Techniques

Although increasing the area of CMOS transistors reduces random offsets [74], achieving sub-millivolt input-referred offsets in CMOS circuits is not practical without using circuit techniques that dynamically compensate the inherent component mismatches. State-of-the-art dynamic offset-cancellation circuits use either auto-zero (AZ) or chopper principles [75-85]. In an auto-zero technique, the offset cancellation is performed in two phases, a *sampling* phase where the offset is measured and sampled and a *normal operation* phase where the sampled offset is subtracted from the input signal. On the other hand, the chopper technique employs modulation instead of sampling to eliminate the offsets. In this technique, a modulator and a demodulator are implemented before the inputs and after the outputs of the amplifier to be compensated, respectively. The modulator and demodulator usually share the same chopping frequency and a low-pass filter is placed after the demodulator outputs. The input signal is processed through modulator, amplifier, and demodulator stages. The inherent offset of the amplifier, however, does not see the modulator. As a result, at the chopper output, while the desired signal is at base band, the offset term is at chopping frequency and at its odd harmonics. Consequently, the signal and offset are separated in the frequency domain and a low-pass filter can be used at the output to remove the offsets.

Although both chopper and auto-zero techniques cancel the offset, their characteristics make them suitable for different applications. While the chopper technique has a continuous-time operation, the basic auto-zero technique can only amplify the signal during the normal operation phase, and it operates discontinuously. However, in

the chopper technique, the bandwidth of the input signal should be limited to half of the chopping frequency (f_{Chop}) to prevent aliasing in the demodulation phase, while there is no limit on the bandwidth of the input signal in auto-zeroing. Moreover, the chopping frequency cannot be increased above a few kilo-Hertz since the offset-cancellation performance of chopper circuits degrades due to residual offsets at high chopping frequency [75]. For a current-sensing application, the input voltage is a pulsatile signal of 1 MHz frequency and significant harmonics up to 10 MHz, which prohibit use of chopper circuits. The characteristics of auto-zeroing and chopper techniques are summarized in Table 6.2.

Table 6.2— Summary of dynamic offset cancellation techniques.

Chopper	**Basic auto-zeroing**
Modulating and filtering the offset	Sampling and subtracting the offset
Continuous-time operation	Discontinuous-time operation
Higher noise-reduction ability	Lower nois-reduction ability
Low bandwidth (BW<f_{Chop}/2)	High bandwidth

There are two methods, known as ping-pong and feed-forward techniques [75-85], discussed in the literature to modify the basic auto-zero circuit and make it continuous. In ping-pong techniques [77-80], as illustrated in Figure 6.4, two identical units are employed, and while one of the units is in sampling phase, the other is in signal path and vice versa. The appearance of spikes and glitches at the output is a practical problem in ping-pong topology, which is the result of disconnecting one unit and connecting the other to the output node at switching time.

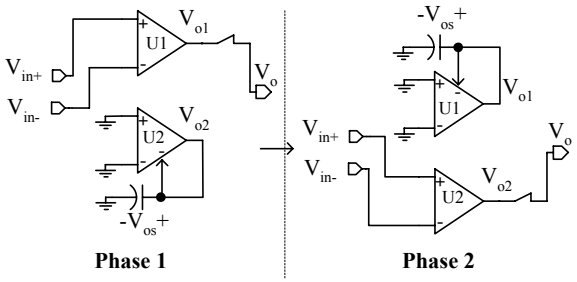


Figure 6.4— The basic continuous auto-zeroing ping-pong technique.

The feed-forward amplifier principle [81-94], as illustrated in Figure 6.5, is subject to fewer spikes and glitches at the output, since no switching happens at the output node. During the first phase, the nulling amplifier measures and cancels its own offset ($V_{os\text{-}n}$). In the second phase, the offset-free nulling amplifier measures the main amplifier offset ($V_{os\text{-}m}$), and removes its effect through the auxiliary port of the main amplifier. Unfortunately, two practical issues limit the use of the feed-forward technique. The feed forward offset-cancelled amplifier is operational only if it is placed in negative feedback and its inputs are kept electrically close to each other, which is not the case for a current-sensing g_m-C filter. Moreover, it suffers from intermodulation effects between the auto-zero clock frequency and the input signal [75, 83, 84], which results in frequency-response distortion. The properties of ping-pong and feed-forward techniques are listed in Table 6.3.

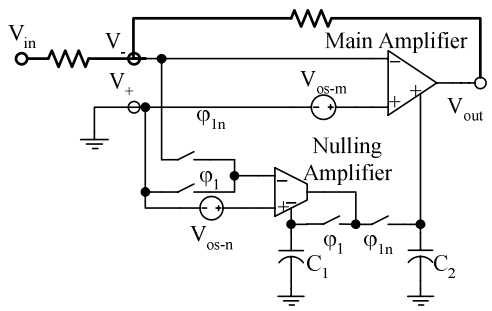


Figure 6.5— Continuous auto-zeroing feed-forward technique.

Table 6.3— Summary of continuous-time auto-zeroing techniques.

Ping-Pong	**Feed-forward technique**
High glitches	Low glitches
Applicable to open-loop and closed-loop amplifiers	A closed-loop negative feedback is required
No intermodulation problem	Intermodulation problem

Proposed Offset Cancellation System

Figure 6.6 illustrates the proposed continuous, low-offset, g_m-C filter, which is realized by applying ping-pong technique to basic g_m-C filter of Figure 6.3. The circuit includes two identical (i.e., well matched) transconductors g_{m11} and g_{m12} and non-overlapping clocks (to prevent cross wiring). While one transconductor processes the

input signal (e.g., for φ equal to ‘’1’’ and φn equal to ‘’0’’, g_{m11}), the other one auto zeroes itself (e.g., g_{m12}) by closing the unity-gain loop through auxiliary input and short-circuiting the main inverting and non-inverting terminals. The measured offset is then stored across the holding capacitor connected to auxiliary port and the input signal is connected to the main input terminals in next phase.

Storing the offset voltage in ac-insensitive nodes, in other words, in remote nodes that do not process the input signal, affords the designer some luxuries. The size of the holding capacitor, for instance, can be increased without affecting the frequency response of the g_m-C filter. In this way, clock feedthrough and charge injection are reduced and offset-cancellation performance is therefore improved [75].

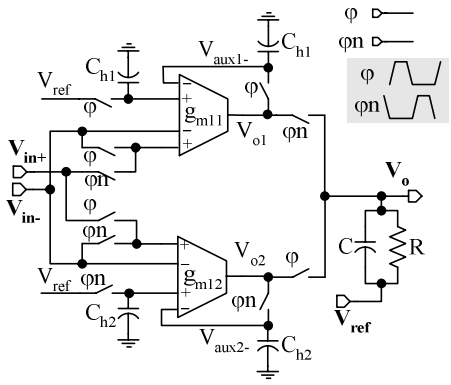


Figure 6.6— The proposed g_m-C filter with ping-pong auto-zeroing.

Analysis of Offset Cancellation

The basic idea in auto-zeroing is to measure the offset in one phase and subtract it from the forward path in the other. Measuring the offset is achieved by disconnecting the amplifier from the output and configuring it for unity gain [75]. In the proposed circuit, a summing transconductor is used to decouple the signal path from the offset holding capacitor (Figure 6.6 and Figure 6.7). The Norton equivalent circuit for the transconductance is shown in Figure 6.7(a) where g_{m1} and g_{ma} are the transconductance values of the main and auxiliary pairs, R_o is the transconductance output impedance, and $V_{Natural}$ is the natural output voltage of transconductance, which is the output voltage of a perfectly matched transconductance g_{m1} when its input pairs are shortened and no load is connected at its output.

In measurement phase, as illustrated in Figure 6.7(b) for only one of the g_m units, the main inputs are shortened and transconductance is placed in unity gain configuration through its auxiliary inputs to evaluate its input-referred offset at its negative auxiliary voltage,

$$V_{aux1-} = \left[\frac{(g_{ma}V_{ref} + g_{m1}V_{os1} + g_{ma}V_{os2})R_o + V_{Natural}}{1 + g_{ma}R_o} \right], \tag{6.1}$$

where V_{os1} and V_{os2} are the input-referred offsets of the main and auxiliary ports and $g_{ma}R_o$ is the loop gain, which is designed to be significantly higher than unity by making R_o very large.

Eventually, sampling phase finishes and normal operation starts. The offset is subtracted from the signal path by reconfiguring the summing transconductor and connecting it to the RC load as shown in Figure 6.7(c). In this phase, the stored offset voltage is applied to the inverting terminal of the auxiliary pair, which was measured in previous phase and is held at capacitor C_h. As a result, the output voltage V_o becomes

$$\begin{aligned} V_o &= (R_o \parallel R)I_o + \left(\frac{R_o}{R+R_o}\right)V_{ref} + \left(\frac{R}{R+R_o}\right)V_{Natural} \\ &= (R_o \parallel R)\left[g_{m1}(V_{in+} + V_{os1} - V_{in-}) + g_{ma}(V_{ref} + V_{os2} - V_{aux1-} + V_{INJ-err})\right], \\ &\quad + \left(\frac{R_o}{R+R_o}\right)V_{ref} + \left(\frac{R}{R+R_o}\right)V_{Natural} \end{aligned} \tag{6.2}$$

where V_{in+} and V_{in-} are positive and negative input voltages and $V_{INJ-err}$ is the clock feedthrough and charge injection errors introduced via switches S_1 and S_2 during the phase transition. Substituting V_{aux1-} calculated in Equation 6.1 into Equation 6.2 results in

$$\begin{aligned} V_o = {} & [g_{m1}(R_o \parallel R)](V_{in+} - V_{in-}) + V_{ref} \\ & + \left[\frac{g_{m1}(R_o \parallel R)}{1 + g_{ma}R_o}\right]V_{os1} + \left[\frac{g_{ma}(R_o \parallel R)}{1 + g_{ma}R_o}\right]V_{os2} \\ & - [g_{ma}(R_o \parallel R)]V_{INJ-err} \\ & + \left[\frac{1}{1 + g_{ma}R_o}\frac{R}{R+R_o}\right](V_{Natural} - V_{ref}) \end{aligned} \quad . \tag{6.3}$$

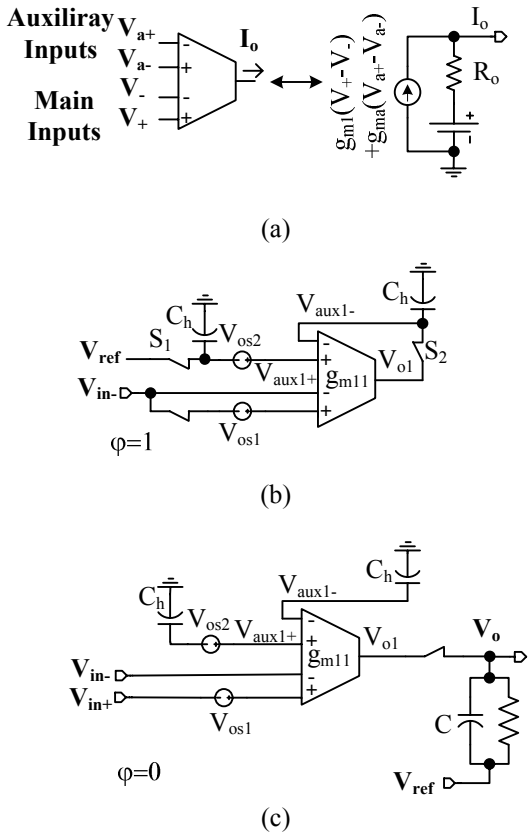


Figure 6.7— Proposed circuit offset-cancellation analyses: (a) Transconductance Norton model, (b) sampling phase, and (c) normal phase.

The first two terms in the right side of Equation 6.3 is the desired output voltage and other terms are errors caused by initial offsets, charge-injection error, and finite gain error to set dc operating point, respectively. Therefore, the equivalent input-referred offset is output-referred errors divided by g_m-C filter dc gain and is equal to

$$V_{os\_eq\_input} \approx \frac{V_{os1}}{g_{ma}R_o} + \frac{V_{os2}}{g_{m1}R_o} - \left(\frac{g_{ma}}{g_{m1}}\right)V_{INJ\text{-}err} + \frac{V_{ref} - V_{Natural}}{(g_{m1}R_o)(g_{ma}R_o)}, \qquad (6.4)$$

where it is assumed that the g_m-cell output resistor R_o, which is a cascoded stage output resistor is much greater than the output resistor (i.e., R_o>>R). As a result, the initial offset terms V_{os1} and V_{os2} are significantly attenuated. The accuracy of the foregoing technique is therefore limited dominantly by charge injection and clock feedthrough errors ($V_{INJ\text{-}err}$), as is the case in most of auto-zeroing schemes [75]. The charge injection and clock feed-though errors can be mainly limited by increasing the size of hold capacitors. Moreover,

difference of $V_{Natural}$ and V_{ref} introduce an error term and affect the input-referred offset. Natural voltage $V_{Natural}$ is a function of supply voltage, input common mode, supply and common mode rejection ratios (i.e., CMRR and PSRR), and topology of the circuit, which limit the effectiveness of dynamic offset cancellation techniques.

Analysis of Transient Spikes

Transient spikes occur in ping-pong auto-zero schemes because at the time of switching the output voltage of subsequently connected unit is not equal to the previously connected one. To study the transition glitches, a transition from when g_{m11} is in signal path to the state where g_{m12} is in signal path is illustrated in Figure 6.8(a) and 6.8(b). Before the transition (Figure 6.8(a)), the circuit output voltage V_o is equal to the g_{m11} output (V_{o1}) and the output voltage follows the g_{m12} output voltage (V_{o2}) after the ping-pong transition (Figure 6.8(b)). Glitches and spikes happen since V_{o1} and V_{o2} are not necessarily equal at the time of transition. While V_{o1} is a function of transconductance gain and bandwidth and input voltage (i.e., $V_{o1}=f(V_{in+}-V_{in-})$), V_{o2} is independent of input voltage, and is usually close to the reference voltage (V_{ref}) used in sampling phase of offset cancellation. Therefore, at the transient time, V_{o2} is not correlated to the input signal and may be off from its desired operation value when connected in signal path. Just after g_{m12} is connected in signal path, the output capacitor charge redistributes and sets the output voltage to somewhere between V_{o1} and V_{o2}, causing an instantaneous error of ΔV_{glitch} (Figure 6.8(c)). After the transition, the circuit corrects the disturbance, and output voltage converges to its desired value with a rate determined by the circuit bandwidth. Assuming that low frequency pole of 1/RC dominates the response, the deviation from ideal output voltage after a switching transition becomes

$$V_{Error} = \Delta V_{Glitch}\left(e^{-\left(\frac{t}{RC}\right)}\right)u(t)\,, \qquad (6.5)$$

where ΔV_{glitch} is the instantaneous glitch.

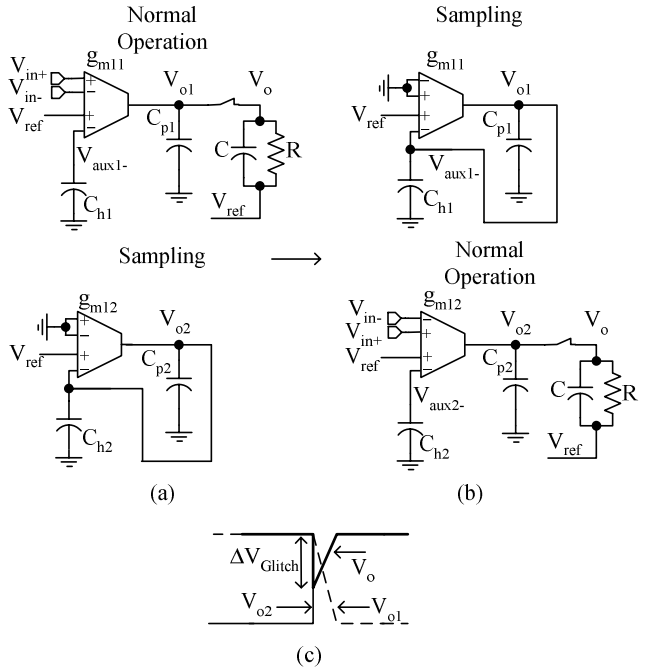


Figure 6.8— Transient glitch analysis: (a) g_{m11} in signal path, (b) g_{m12} in signal path, and (c) transient response.

The value of ΔV_{Glitch} can be quantified by investigating charge redistribution at the transient time. Just before the transition, output voltage at capacitor C is equal to the g_{m11} output voltage and a function of input voltage (i.e., $V_o=V_{o1}=f(V_{in+}-V_{in-})$). At the same time, V_{o2} is close to V_{ref} assuming initial mV offset voltage are much smaller than V_{ref}, which is in the order of Volts. As a result, the g_{m12} output capacitor C_{p2} is charged to V_{ref}. During hand-over event, first, the output capacitor C and resistor R are disconnected from V_{o1} and g_{m12} negative auxiliary input is disconnected from V_{o2}, and, then, the output capacitor C and resistor R are connected to V_{o2}. Consequently, capacitors C_{p2} and C with different voltages are connected together and charge redistribution happens between them, which can be described as

$$\begin{aligned} &Cf(V_{in+}-V_{in-})+C_{p2}V_{ref} \\ &\quad = C\left(f(V_{in+}-V_{in-})+\Delta V_{glitch}\right)+C_{p2}\left(f(V_{in+}-V_{in-})+\Delta V_{glitch}-V_{ref}\right). \end{aligned} \quad (6.6)$$

Therefore, the output voltage glitch becomes

$$\Delta V_{glitch}=\left(\frac{C_{p2}}{C+C_{p2}}\right)\left(f(V_{in+}-V_{in-})-V_{ref}\right). \quad (6.7)$$

Since output capacitor C is much larger than parasitic capacitor C_{p2}, the output glitches are significantly reduced. For a filter capacitor C of 60 pF, 1.33 pF of C_{p2}, and 0.8 V worst-case difference between V_{ref} and output voltage V_o (V_o=f(V_{in+}-V_{in-})), the glitches are theoretically limited to 17 mV.

Circuit Implementation

Programmable Transconductance G_{m1}

High linearity, rail-to-rail input common-mode range (ICMR), programmability, high output resistance, and an auxiliary transconductance path for offset cancellation are the key design parameters of the transconductor. The topology proposed, as illustrated in Figure 6.9, is derived from a second-generation current conveyor (CCII) [86], where a resistor (R_1) is connected in series with the inverting input of a unity-gain amplifier. Shunt feedback ensures that the impedance at the source of M_3 is low [86, 87]. The input voltage across resistor R_1 (differential input voltage across the transconductor) causes current I_{R1} to flow into it, and

$$I_{R1} = \frac{V_+ - V_-}{R_1}, \tag{6.8}$$

where V_+ and V_- are positive and negative main terminal inputs. This current and bias current I_b are summed and mirrored by M1-M2, which subtracts it from another bias current I_b at the output, resulting in a bi-directional output current whose magnitude is linearly proportional to the differential input voltage and inversely proportional to R_1.

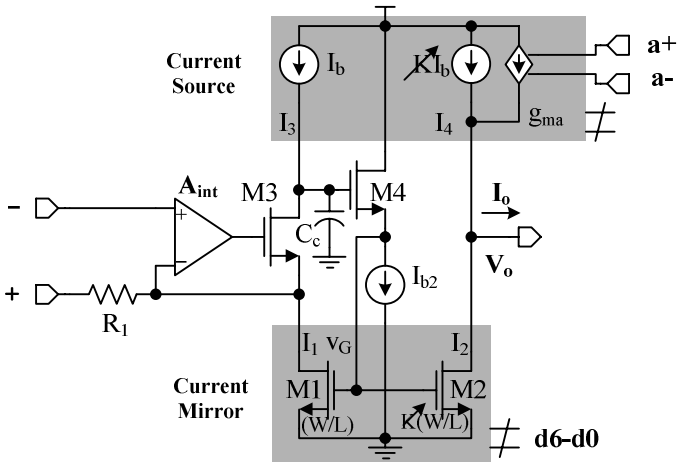


Figure 6.9— Simplified circuit block diagram of transconductance g_{m1}.

The feedback loop around device M1 (M1, common-gate M3, and source-follower M4) is used to bias and decouple the gates of current mirror M1-M2 from node 2, which partially defines the ICMR of the transconductor. Capacitor C_c sets the dominant pole frequency of that loop. In closed loop, the mirror adds a high frequency parasitic pole to the filter, at its unity-gain frequency (gain-bandwidth product) – $g_{M1}/C_{c,}$ where g_{M1} is the transconductance of M1. Amplifier A_{int} is a standard PMOS input, two-stage, Miller-compensated amplifier with a gain-bandwidth product of 10 MHz.

The programmability feature is added by digitally controlling the gain of the current-mirror and more specifically, by programming the connectivity of a binarily weighted array of current mirrors (Figure 6.10(a)). For example, if bit d_i is low, the gate of cascode transistor N_i is connected to ground and the i^{th} mirror is disabled; otherwise, it is connected to a bias voltage and therefore enabled. Since the mirror amplifies both I_{R1} and DC bias current I_b, an equally gained DC bias current is sourced to the output, resulting in a net DC and ac bidirectional current gain of K and therefore a net transconductance of

$$g_{m1} = \frac{K}{R_1}. \tag{6.9}$$

Cascoding transistors are added to the current mirrors and sources to increase the output resistance of the transconductor.

The auxiliary transconductance input path (g_{ma}) used for offset cancellation is realized by summing a voltage-controlled current source to the output of the aforementioned circuit, as shown in Figure 6.10(b). For functional efficiency, the bias current generator and this auxiliary path are combined into a single circuit. Transistor pairs Pa-P1 and Pb-P2 form current sources. Current-canceling differential pair N_a-N_d is used to generate low transconductance values [89]. The resulting transconductance of the auxiliary path is

$$g_{ma} = K(g_{mad}), \tag{6.10}$$

where g_{mad} is the transconductance of the composite differential pair N_a, N_b, N_c, and N_d. Amplifier A_2, which is a conventional single-stage amplifier, forces the drain voltages of transistors P1 and P2 to be equal, thereby mitigating channel-length modulation effects and improving accuracy performance.

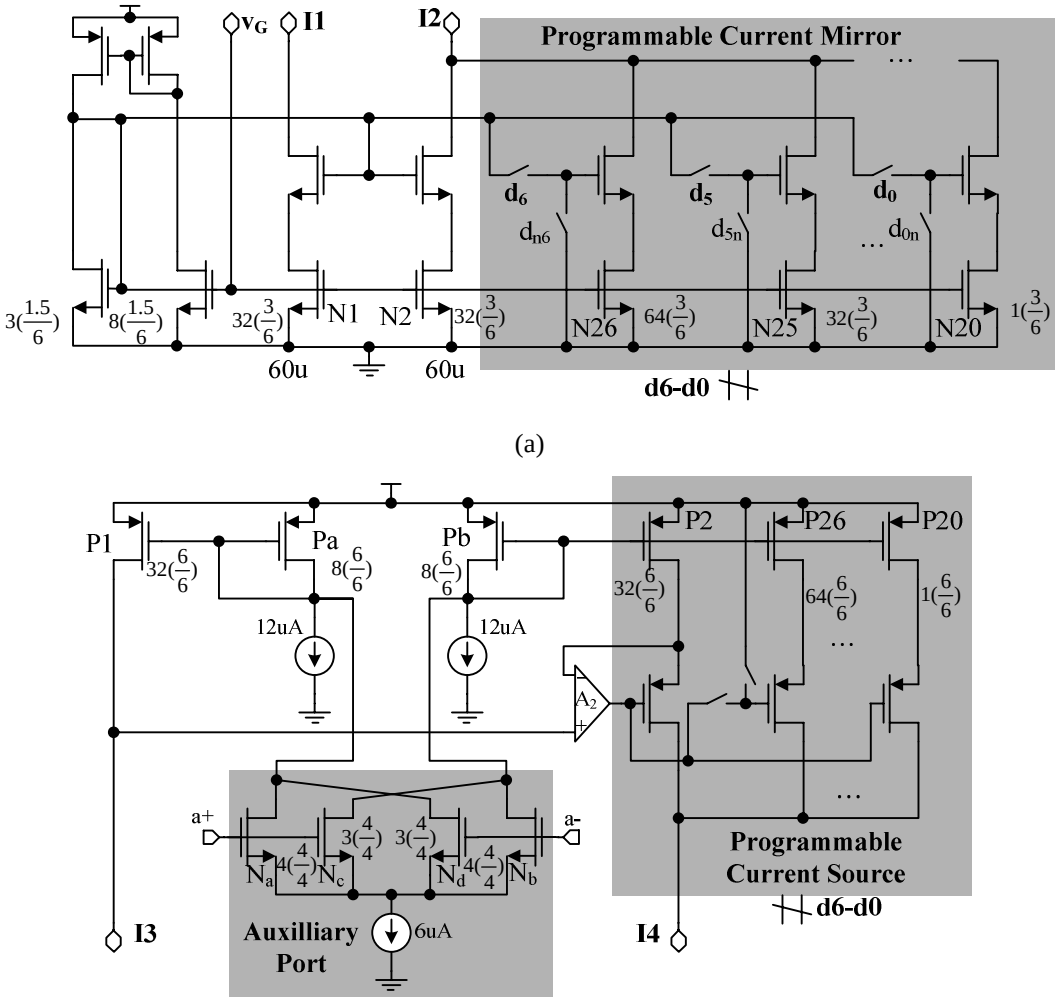


Figure 6.10—Proposed g_m-cell components: (a) programmable current mirror and (b) programmable current source with auxiliary inputs.

High linearity is required to prevent systematic offsets at the output for pulsatile rail-to-rail input signals. For example, for a rail-to-rail, 50% duty cycle input at V_{in+} and a constant input at half of the rail at V_{in-}, a nonlinearity Δg_m causes average value of output voltage of g_m-C filter to deviate from ideal zero to

$$\begin{aligned} V_o &= (g_{m1} + \Delta g_{m1})R(V_{DD} - V_{DD}/2) + (g_{m1})R(-V_{DD}/2) \\ &= (\Delta g_{m1}R)\left(\frac{V_{DD}}{2}\right) = (g_{m1}R)\left(\frac{\Delta g_{m1}}{g_{m1}}\right)\left(\frac{V_{DD}}{2}\right) \end{aligned} \quad . \qquad (6.11)$$

As a result, transconductance nonlinearity causes a systematic input-referred offset of

$$V_{os\_sys} = \left(\frac{\Delta g_{m1}}{g_{m1}}\right)\left(\frac{V_{DD}}{2}\right). \qquad (6.12)$$

To prevent systematic offsets, the transconductance g_{m1} should have high linearity, which is achieved through amplifier A_1 and feedback around resistor R_1. Therefore, the dominant source of nonlinearity is the NMOS current mirror that is taken care of by selecting large bias current compared to resistor R_1 current (I_b>10max(I_{R1})). However, using high bias currents introduces a tradeoff, since they increase thermal noise.

Tunable resistor R

The bandwidth of the g_m-C filter is tuned via a high-resistivity (1 KΩ/□) poly resistor (R in Figure 6.3), which is, again, realized by digitally re-arranging the connectivity of a binary weighted resistor array (Figure 6.11). Switches S_0-S_7 are NMOS transistors with aspect ratios 20 times larger than the minimum size allowed to ensure their respective switch-on resistances are low enough not to affect the resolution of the array. It is noted that this scheme is not applied to make resistor R_1 (Figure 6.9) because the parasitic capacitors of the switches degrade the overall frequency response of the filter. These parasitic capacitors, on the other hand, have negligible effects when applied to R because the dominant low frequency capacitor C also resides on that node, in parallel with R.

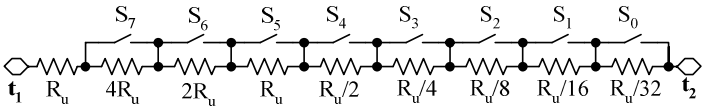


Figure 6.11— The adjustable resistor.

Experimental Results

The proposed g_m-C filter was designed and fabricated in AMI's 0.5 µm CMOS process technology. The G_M-C filter die photograph is illustrated in Figure 6.12 and its top-level design parameters are summarized in Table 6.4. Transconductance-setting resistor R_1 is 250 kΩ, bandwidth-setting capacitor C is 60 pF, mirror-gain range is 1 to 5 with seven bits of resolution, bandwidth-setting resistor range is 325 to 2,900 kΩ with eight bits of resolution, and the auto-zeroing clock frequency is 1 kHz. The DC gain and

bandwidth of the filter were adjustable from 1.27 to 29.16 V/V and 1.1 to 6.4 kHz, respectively, partial experimental results of which are shown in Figure 6.13.

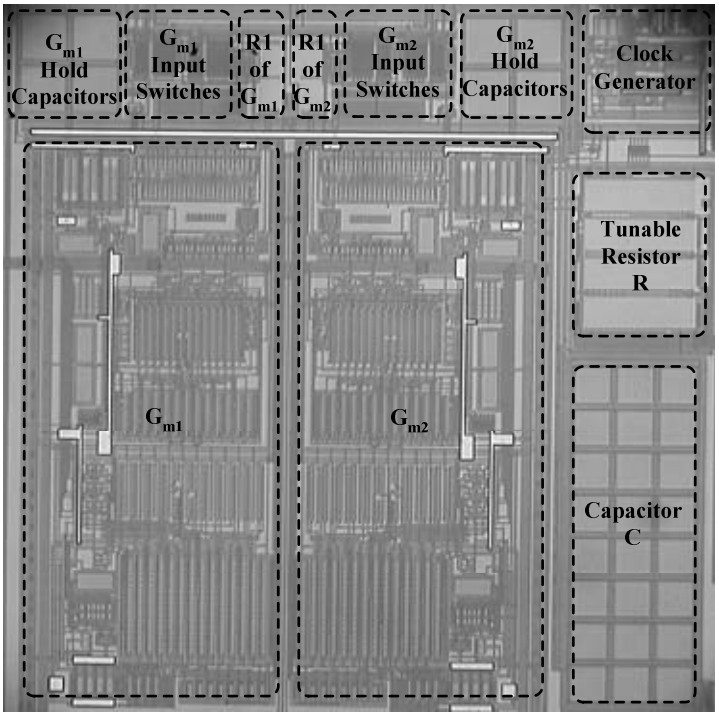


Figure 6.12— Chip photograph illustrating g_m-C filter layout.

Table 6.4— G_m-C filter key design parameters.

Specification	Value
Resistor R_1 of g_m	250 kΩ
Mirror Ratio (g_{m_max}/g_{m_min})	5
g_m Resolution (Δg_m)	$(1/32)g_{m\_min}$
Resistor R	325 kΩ-2900 kΩ
Resistor R Ratio (R_{max}/R_{min})	9
R Resolution (ΔR)	$(1/32)R_{min}$
Capacitor C	60 pF
Hold Capacitors C_{h1} and C_{h2}	6 pF
Auto-Zero Clock Nominal Frequency	1 kHz

The g_m-C filter was subjected to the low impedance rail-to-rail signal generated by a current-mode switching buck regulator circuit and used to sense and control the

regulator's current-mode feedback. The experimental transient results are illustrated in Figure 6.14, and as expected, the square wave is integrated into a triangle by the g_m-C filter. The ping-pong "hand-over" event referred to in the transient glitch analysis section of this paper is highlighted in Fig. 6.14(b) and shown to be less than 40 mV for worst-case DC output voltage conditions (i.e., largest V_o-to-V_{ref} voltage difference). Although the resulting transient glitch effectively changes the duty cycle of the converter (because its output is used, in part, to control the switching supply), its net effect is negligible and easily compensated within one switching cycle.

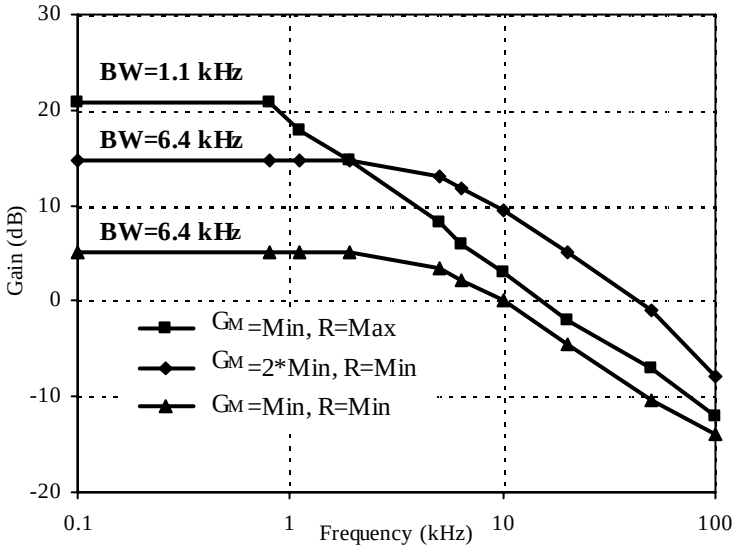


Figure 6.13— Measured frequency response of the g_m-C filter.

To verify the offset cancellation capability of the circuit, one of the transconductors was disabled and the other observed, short-circuiting the input and monitoring the output of the transconductor before (V_{o1} in Figures 6.6 and 6.7) and after it is connected to bandwidth-setting capacitor C (V_o) via on-chip buffers, as shown in Figure 6.15. The peak-to-peak voltage of V_o represents the cumulative output-referred offset voltage of the summing transconductor because V_o is clamped to V_{ref} when disconnected from the transconductor and auto-zeroed to V_{ref} - $V_{os}g_mR$ when connected. The resolution of the oscilloscope was unfortunately limited to approximately 5 mV,

limiting the resolution of the measurement to approximately 500 µV (5 mV / 9.92 V/V) of input-referred offset.

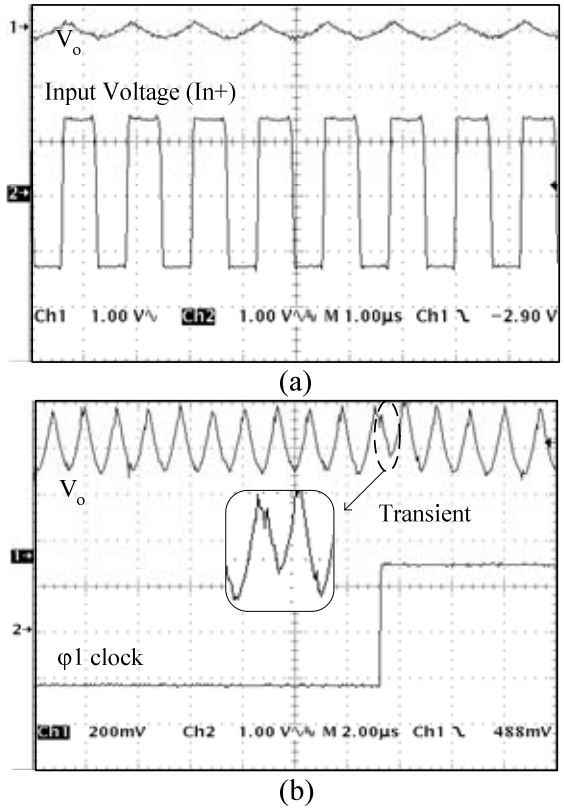


Figure 6.14— G_m-C filter response to a rail-to-rail input pulse signal: (a) steady state and (b) during a hand-over event.

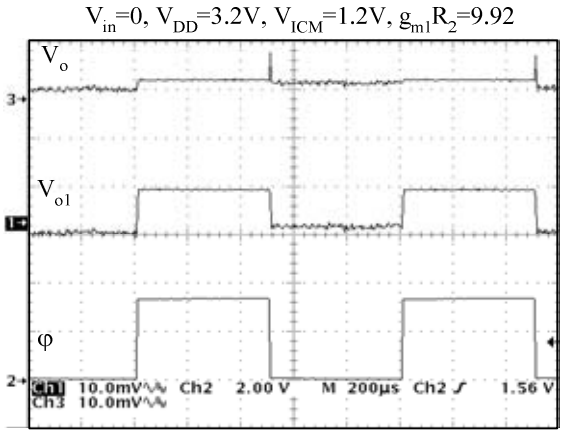


Figure 6.15— Illustration of offset-cancellation mechanism in g_m-C filter.

To improve the accuracy of the measurement, the output of the g_m-C filter and therefore the offset of the same were amplified on-chip by 26 dB before measuring it with the oscilloscope, as shown in Fig. 6.16. Consequently, when g_m-C output V_o is disconnected and clamped to V_{ref}, both inputs of the amplifier in the gain stage are at V_{ref} and the output is therefore zero. However, when the auto-zeroed transconductor is connected, the output voltage difference to V_{ref} is amplified and measured. The clocking sequence of the test setup was as follows: (1) g_m-C filter inputs are short-circuited on-chip and transconductor 1 is auto-zeroed, (2) auto-zero is disabled and transconductor is connected to bandwidth-setting capacitor C with g_m-C filter inputs still short-circuited on-chip, and (3) g_m-C filter inputs are disconnected on-chip but reconnected off-chip. The 40 μV (8 mV divided by the g_m-C filter's gain of 9.92 and pre-amplifier gain of 20) difference between phase 2 and phase 3 input voltages occurs since off-chip short-circuit condition is not ideal, and phenomena such as thermocouple effect can cause non-zero input voltage at the input of transconductance during offset measurement phase. Since the circuit is designed to filter the voltage across an off-chip inductor, the voltage difference between the first and third phases of the clocking sequence is the output-referred offset voltage of the transconductor. Since the offset of the additional gain stage is common-mode to all phases and only the differential voltage between phases is measured, the preamplifier's input-referred offset has no effect on the accuracy of the measurements. The amplified output-referred offset under various conditions (power supply of 3 and 4.2 V and input common-mode range of 1, 1.2, and 1.5 V) are shown in Figure 6.17. The resulting input referred offset for three samples was less than ± 210 μV (42 mV divided by the G_M-C filter's gain of 9.92 and pre-amplifier gain of 20).

The circuit was operational for auto-zeroing clock frequencies ranging from 10 Hz to 10 kHz (Figure 6.18). At higher frequencies, the auto-zeroing properties were diminished because the circuit does not have enough time to settle to its auto-zeroed value. On the other extreme, the hold capacitors limit the amount of time the auto-zeroed voltage is held in the presence of leakage currents from parasitic reverse-biased junction diodes, which is why 10 Hz is the lower limit for this circuit. Since DC offsets are nothing more than low frequency signals, dynamic offset-cancellation schemes also reduce 1/f low frequency noise. Given the low bandwidth nature of the g_m-C filter, output

noise is further reduced, and in the foregoing case, the total input-referred noise was measured to be 93 μV with a filter DC gain of about ten at R_{Max}. The circuit's nonlinearity performance ($\Delta g_m/g_m$) was found to be -57 dB by measuring the resulting common-mode input-induced systematic offset for a rail-to-rail non-inverting input signal. Table 2 summarizes the other performance parameters of the circuit.

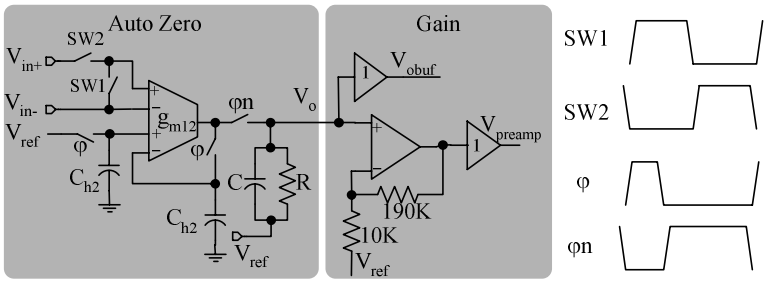


Figure 6.16— G_m-C filter offset measurement test setup. Measurements are performed at V_{preamp}. The preamplifier with gain of twenty is added at the output to increase measurement resolution.

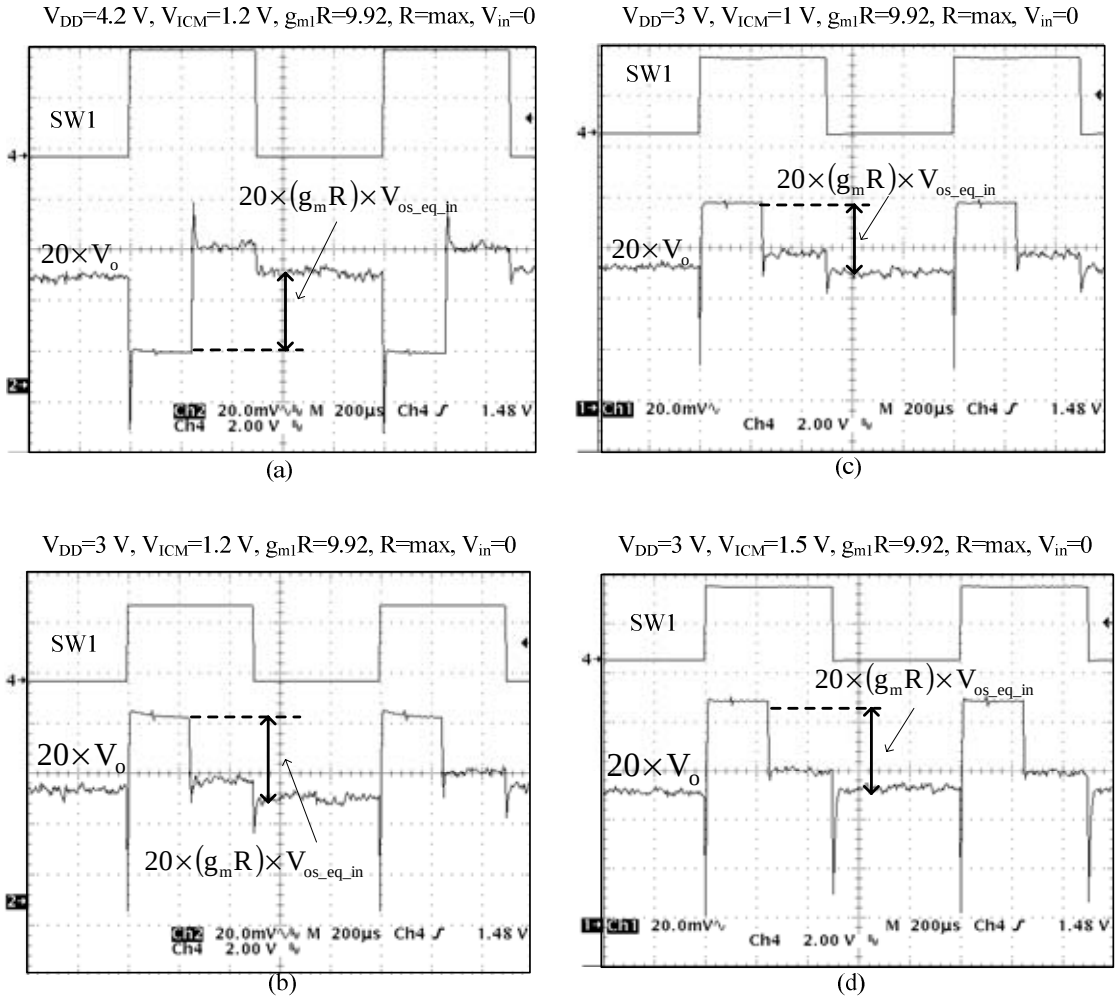


Figure 6.17— G_m-C filter output measurement under extreme supply and input common mode ranges: (a) V_{DD}=4.2 V, V_{ICM}=1.2 V, (b) V_{DD}=3 V, V_{ICM}=1.2 V, (c) V_{DD}=3 V, V_{ICM}=1 V, and (d) V_{DD}=3 V, V_{ICM}=1.5 V.

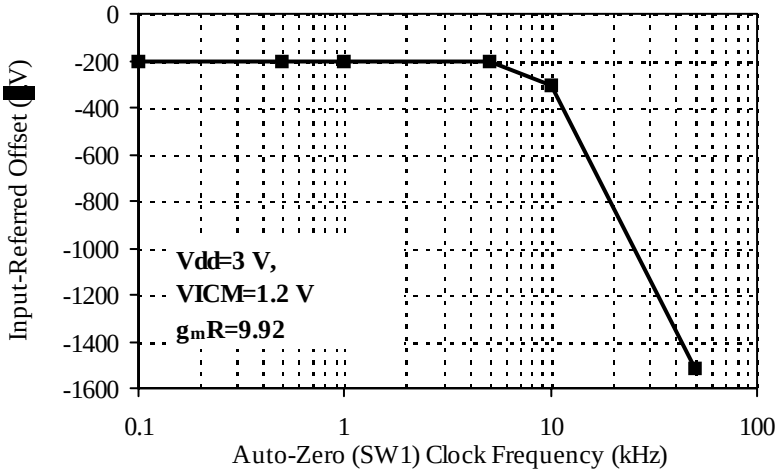


Figure 6.18— Input-referred offset of g_m-C filter versus auto-zeroing clock frequency.

<u>*Conclusions*</u>

A programmable and linear low offset 0.5-μm CMOS g_M-C filter has been proposed, designed, fabricated, and evaluated. The experimental offset was measured to be less than ± 210 μV for 3 to 4.2 V supply voltages (lithium-ion battery supply range) and 1 to 1.5 V input common-mode voltages. The DC gain and bandwidth were adjustable from 1.1 to 6.4 kHz and 1.27 to 29.16 V/V, respectively, both with better than 3.2 % resolution by adjusting the transconductance via the gain of a current mirror and the resistance of a shunting bandwidth-setting resistor. "Hand-over" glitches during ping-pong transitions were less than 40 mV while achieving a nonlinearity performance of -57 dB. The low input-referred offset, high linearity, continuity, and programmable features achieved with this design are appealing to a growing number of high performance analog systems, from power-moded switching power supplies to front-end interface electronics for telemetry applications, and all under the constraints of CMOS integration. Analog filters, however, which are prevalent in most, if not all, applications that interface with the real world, benefit the most from these performance characteristics.

Table 6.5— Specification compliance matrix of g_m-C filter.

Pins and Parameters	Target	WC Sim.	Expr.	Notes
Power Supply (V_{DD})	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V - 4.2V	
ICMR IN+	-1 V - V_{DD}	-0.6 V V_{DD}	-0.4 V - V_{DD}	Rail to rail
ICMR IN-	0.8 V - 1.6 V	0.8 V - 1.6 V	0.5 V - 1.6 V	WC, 2.7 V supply
OCMR	0.7 V - 2 V	0.75 V - V_{DD}-0.7V	0.7 V - 1.4 V	
VGND	1.35 V	1.35 V ±11mV	1.35 V ±6mV	Experimental results based on five samples
Input-Referred Offset (3σ)	<500 μV	<±500 μV	<±210 μV	Test conditions: V_{DD}=3 V-4.2 V ICR=1 - 1.5 V Filter DC gain=9.92
Output Glitch	<20 mV	17 mV	40 mV	Worst case at minimum output voltage 0.7V
Linearity ($\Delta g_m/g_m$) (Rail-to-rail IN+)	-67 dB	-67 dB	-57 dB	Worst case sim. for 10 mV, ΔV_{Th} offset, 125°C, 2.7 V
Second Pole $f_{switching}$=1 MHz	>8 MHz	8 MHz	4 MHz	Worst case sims for 125°C, I_{bias}-10%
BW Range	1 kHz 5 kHz	1 kHz 8.1 kHz	1.1 kHz 6.4 kHz	
BW Resolution(1) (WC) (Mid range)	3.125% 0.7%	3.125%	NA	Worst-case resolution for Min resistor R
DC Gain Range	2.65 – 44	1.3 - 52.8	1.27 - 29.2	Partially tested Limited test bits at pins
DC Gain Resolution(2) (WC) (Mid range)	3.125% 1.25%	3.125%	NA	Worst-case resolution for Min g_m
Quiescent Current		624 μA 1.2 mA	NA NA	g_m=Min g_m=Max

(1) $\Delta R=(1/32)R_{min}$, $(R_{max}/R_{min})=9$, $R_{mid}=4.5$
(2) $\Delta g_m=(1/32)g_{mmin}$, $(g_{m\_max}/g_{m\_min})=5$, $g_{m\_mid}=2.5$

6.2.2. Tuning

The simple block diagram of the proposed tuning loop, which adjusts the filter high-frequency gain at start-up, is illustrated in Figure 6.19. During the tuning phase, a triangular current with an operational frequency much higher than the inductor cutoff frequency, R_{ESR}/L, is forced into the inductor (i.e., 100 kHz versus 1 kHz). At this high frequency, the inductor's R_{ESR} is much smaller than inductor impedance ($L\omega$) and the g_m-C filter capacitor impedance ($1/C\omega$) is much lower than resistor R. As a result, for high frequency input signals, the transfer function from the inductor current to the output sense voltage becomes

$$V_{Sense\_Tune} = \left(\frac{g_m L}{C}\right) I_L \,. \tag{6.13}$$

Consequently, the output of the g_m-C filter is a triangular signal similar to the test current. The signal at the output of g_m-C filter is amplified with a gain stage, and its AC part is compared to a constant voltage V_{Tune}. Therefore, the output of comparator CMP is activated if the peak value of the triangular signal at the output of the preamplifier exceeds the constant voltage V_{Tune}. The loop adjusts the transconductance g_m such that the preamplifier output peak becomes V_{Tune} or equivalently,

$$\left(\frac{g_m L}{C}\right) K I_p = V_{Tune}\,, \tag{6.14}$$

where K is the preamplifier gain, and I_p is the peak value of the triangular test signal. The preamplifier is used to amplify the output of the current-sensing filter since filter output during start-up is small because the test current during start-up is much smaller than inductor current during normal operation of the switching regulator. The small test current is a result of practical limitations such as die area that can be dedicated to the current-generator block. The tuning loop operates as follows. A clock gradually increases the output of a counter, which its outputs are connected to the switches that digitally control the value of transconductance g_m. The tuning starts with a reset of counter that sets transconductance g_m at its lowest value. After the reset, at each clock positive edge, the value of transconductance g_m increases. While the transconductance g_m is lower than the desired value, the comparator output CMP is disabled. Eventually, transconductance g_m becomes large enough that the peak voltage of the signal at the output of the preamplifier exceeds V_{Tune}. Then, the output of the comparator CMP trips and stops the counter at a transconductance g_m that satisfies Equation 6.14.

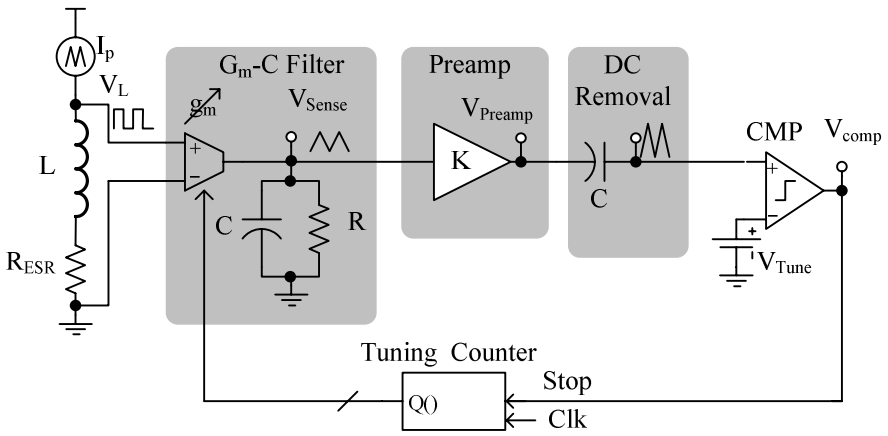


Figure 6.19— Basic block diagram of tuning loop.

The detailed circuit implementation of the tuning block is shown in Figure 6.20. During tuning and calibration, only one of the two transconductance units of the ping-pong g_m-C filter is activated. The preamplifier is implemented using a two-stage amplifier topology for a flat gain of 20 (<0.1 dB gain error) up to five times the triangular test-signal frequency (i.e., 5×200 kHz). The comparator is also two-stage but with a relatively low-gain first stage. The comparator is designed for a delay of about 40 ns for a 10 mV input overdrive. Furthermore, the comparator is unity-gain stabilized with a capacitor at its output since the comparator is placed in a unity-gain feedback in some phases of its operation. The DC-removal circuit is implemented with a high-pass filter with R_f = 1 MΩ and C_{h21} = 8 pF (i.e., 20 kHz 3-dB bandwidth). To reduce AZ_CMP offset, a dynamic offset-cancellation circuit is realized around it using the storage capacitor C_{h22}.

The digital core block starts the tuning phase by activating the *Tune_RST* and *Tune_EN* signals. The Tune_RST is a short pulse that resets the tune-counter to its lowest value at the start of tuning cycle but Tune_EN remains on until Tune_stop is toggled high. The auto-zeroing clocks SW1, SW2, φ1, and φ1n control the operation during tuning and their circuit implementations are discussed in subsection 6.2.4. Although φ1 and φ1n are the same signals as SW1 and SW2, respectively, during tuning and normal operation, they are different during calibration and therefore are distinguished. When SW1 is “1” and SW2 is “0” , the g_m-C filter inputs are connected together and the AZ_CMP inputs are connected to V_{ref} voltage and both are in offset measurement phase.

In the next phase, SW1 becomes “0” and SW2 is “1”, and the g_m-C filter, preamplifier, and comparator are in amplification phase. During this phase, if the peak value of signal at positive input of the comparator exceeds V_{Tune}, pulses appear at inverted output of AZ_CMP, CMPO. These pulses trigger a 3-bit counter and set Tune_stop if more than eight peaks are detected in a single phase. The 3-bit counter is placed to prevent false Tune_stop events that may happen because of noise. Once the Tune_stop signal is activated, the digital core detects it and disables tuning by setting Tune_EN low. However, if Tune_stop is not asserted, the tuning counter increases at the next positive edge of SW1, which increases the g_m-C filter high-frequency gain. The tuning operation continues until Tune_stop is asserted or the tuning counter reaches its highest count.

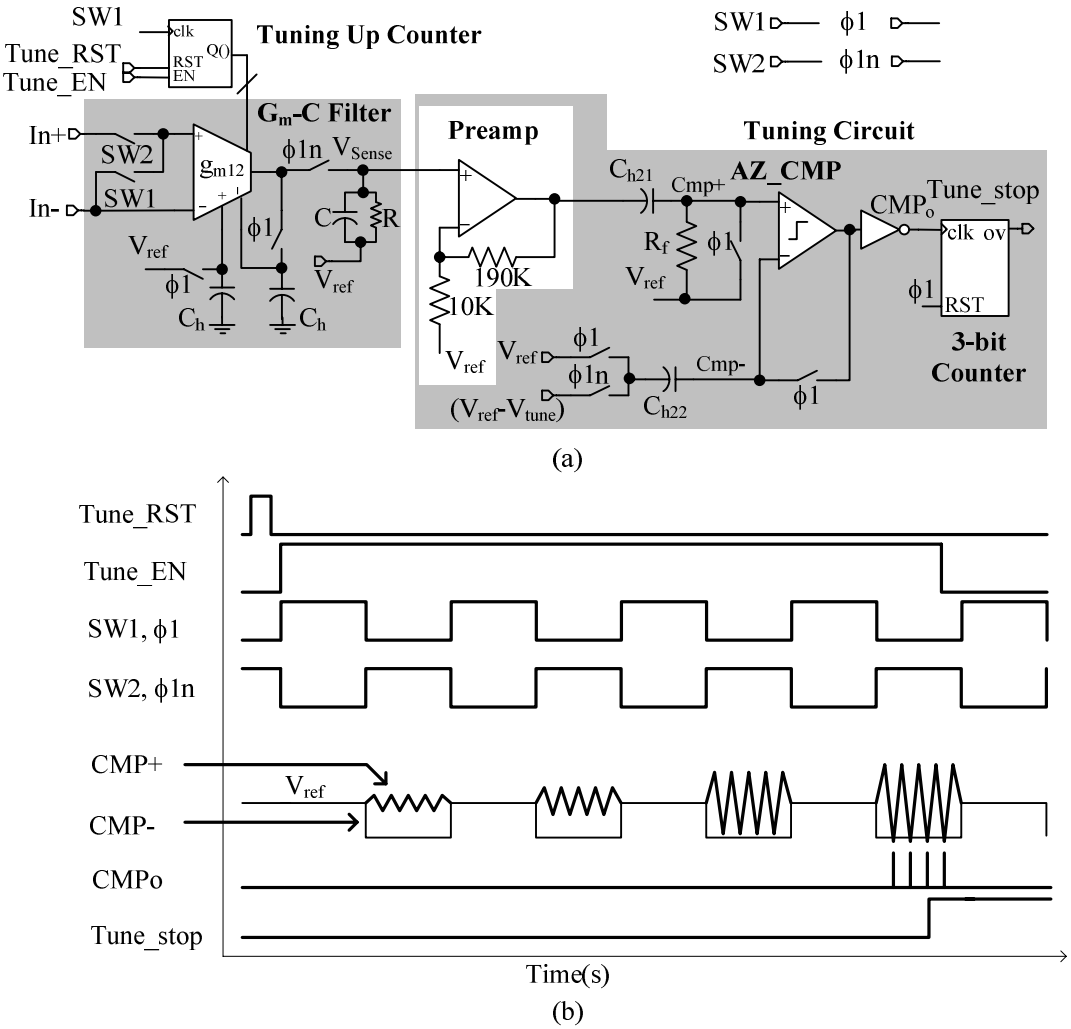
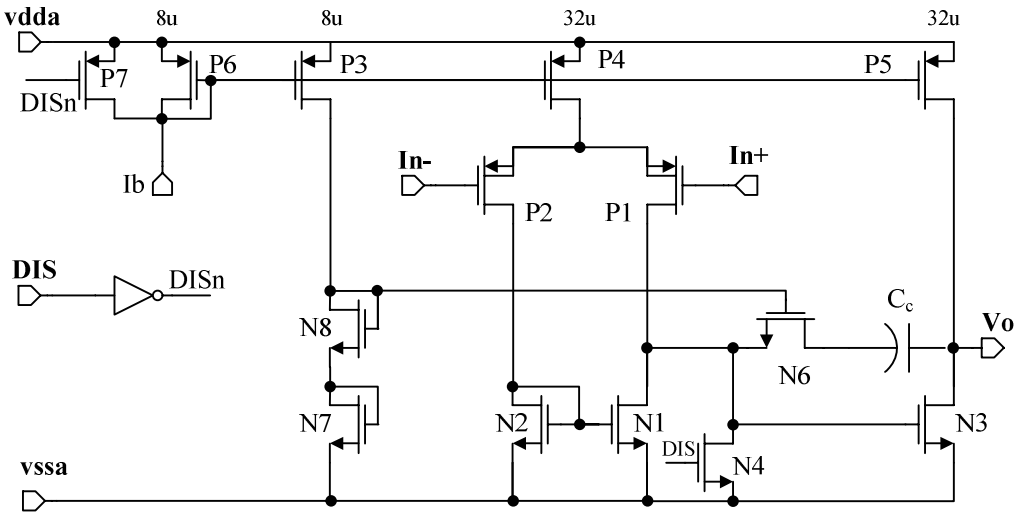


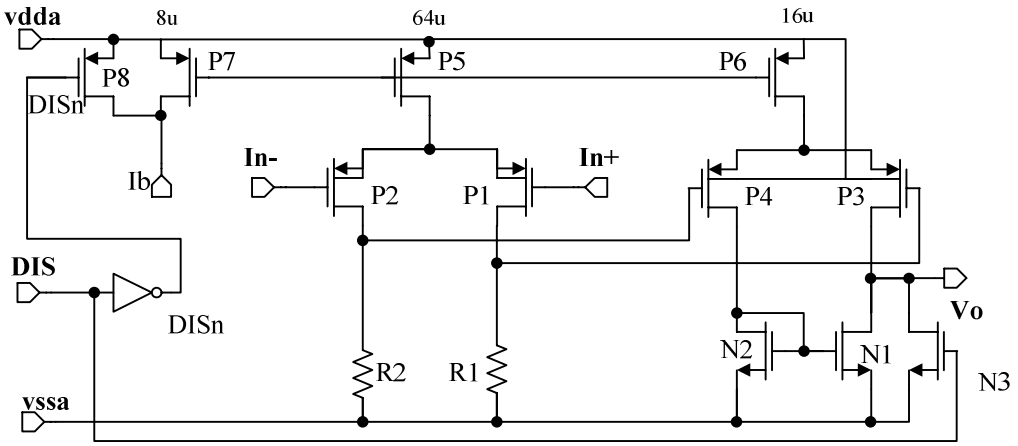
Figure 6.20— Tuning circuit: (a) implementation and (b) waveforms.

The detailed implementations of the preamplifier and comparator circuits are illustrated in Figures 6.21 and Figure 6.22, respectively. The tuning circuit is a two-stage amplifier [89], which is designed to be stable for a feedback gain of 20. The comparator uses a preamplifier gain stage of about five before a five-transistor gain stage of about 100. Since the comparator is put in a unity-feedback gain during the offset measurement phase, it is designed to be stable when it is placed in a unity feedback gain configuration and it is compensated with a 8-pF capacitor of C_{h22} at its output (Figure 6.20).



P1	P2	N1	N2	N6	N3	C_c
4(15/2)	4(15/2)	4(5/4)	4(5/4)	(5/4)	8(5/4)	0.25 fF
P6	**P4**	**P3**	**P5**	**N7**	**N8**	
2(12/4)	8(12/4)	2(12/4)	8(12/4)	2(5/4)	2(5/4)	

Figure 6.21— Tuning/calibration preamplifier circuit.



P1	P2	R1	R2	N1	N2	P3	P4
4(15/2)	4(15/2)	20k	20k	2(5/4)	2(5/4)	2(15/2)	2(15/2)

Figure 6.22— Tuning and calibration AZ_CMP comparator circuit.

Figure 6.23 shows the experimental waveforms of the tuning circuits. Figure 6.23(a) illustrates the triangular generator output and the voltage at the phase node during tuning, where a triangular test current forces a pulsative voltage across the inductor. Figure 6.23(b) and 6.23(c) show the g_m-C filter output, SW1 auto-zeroing clock, and Tune_stop (i.e., processed tuning comparator output). If transconductance high-frequency gain (i.e., g_m/C) is not enough, the comparator output is zero, and Tune_stop is disabled as shown in Figure 6.23(b). However, when the tuning loop locks (i.e., g_m has increased enough), a train of pulses appears at the Tune_stop output where its period is eight times the triangular test signal-period as a result of using a 3-bit counter to deglitch and filter out the output of tuning comparator and prevent noise to enable Tune_stop before proper gain is achieved. Figure 6.24 illustrates the buck converter output voltage V_{out} and wave generator triangular output when tuning starts. Table 6.6 summarizes the performance of the tuning circuit characterized with simulations and measurements.

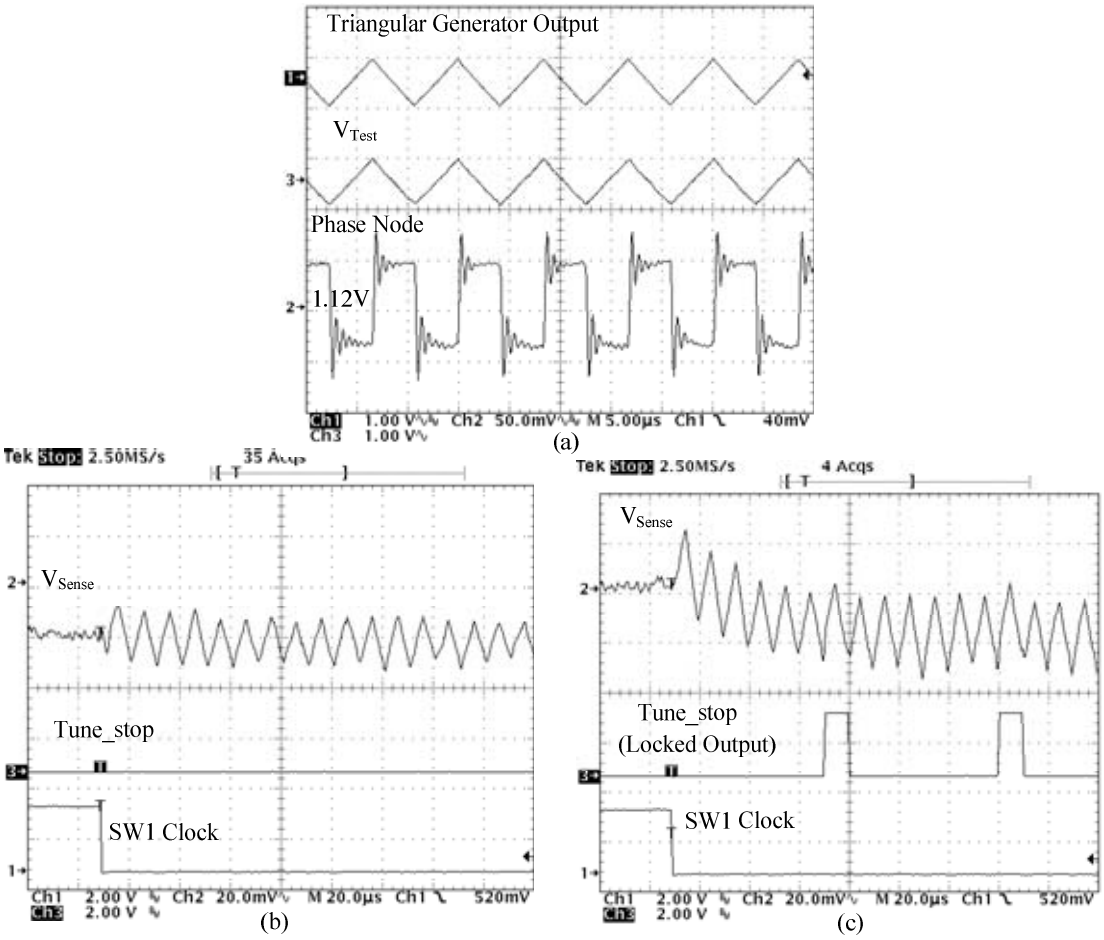


Figure 6.23— Tuning waveforms (a) current-generator and power stage, (b) Tuning loop searching (low g_m), and (c) Tuning loop locked (g_m limit is reached).

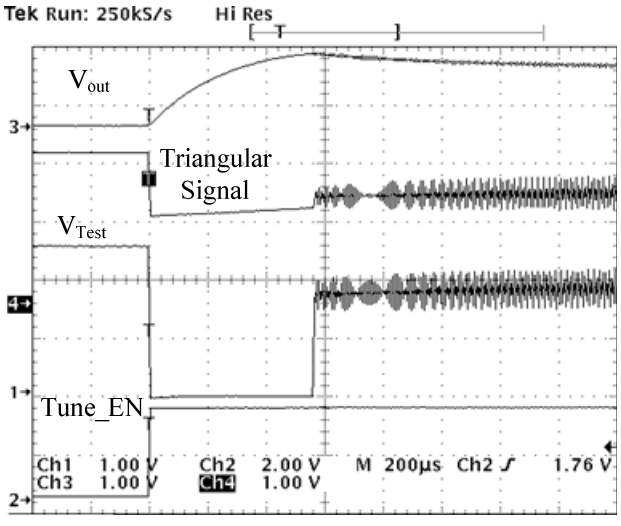


Figure 6.24— Tuning start-up waveforms.

Table 6.6— Specification compliance matrix tuning loop.

Spec. Comp.	Target	Sim.	Expr.	Notes
Target AC Gain	0.5 V/A	0.5 V/A	0.5 V/A	
Total Error	<±4.5%	<±4.5%	-9%	4-bit resolution for AC current detection
Triangular Test Current	25 mA DC 25 mA Peak	35 mA DC 25 mA peak	35 mA DC 25 mA peak	
Supply Voltage	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V - 3.5 V	
Error Budget Details				
Pre-Amplifier Gain Error	<±0.5%	-1.5%	NA	Including gain up to $5\times f_{Triagnular}$
Input Offset Error	Negligible	Negligible	Negligible	High-pass filter is used
V_{ref} + CMP Offset Errors	<±0.5%	<±0.5%	NA	
I_p error (R_{ref})	<±2%	-1%	<±1%	More error in tuning is expected due to the cap.
Quantization Error	±1.5%	±0.75%	NA	Typical values for g_m at its mid range
Filter Second Pole Error	-1%	-2%	-5%	
Total Error	±3.125%	-4.5% ± 1.25%	-9%	

6.2.3. Calibration

The basic block diagram of the calibration phase, which adjusts the filter DC gain during the startup is illustrated in Figure 6.24. In this phase, which starts when tuning phase is completed, a DC current is forced into the inductor (Figure 6.25). Therefore, the resulting voltage across the inductor and the output of g_m-C filter are DC signals. The g_m-C filter output is then amplified through a preamplifier Preamp, and the preamplifier output is forced to be equal to a constant voltage V_{Cal} by changing transconductance g_m through the feedback loop or equivalently,

$$(R_{ESR} I_{DC})(g_m R)K = V_{Cal}, \tag{6.15}$$

where I_{DC} is the calibration DC test current and R is the g_m-C filter resistor. A procedure similar to that discussed in tuning can be used to implement the calibration loop with a counter controlling the resistor R value. If calibration and tuning voltages and test currents are designed to satisfy

$$\frac{V_{Tune}}{I_p} = \frac{V_{Cal}}{I_{DC}}, \tag{6.16}$$

the g_m-C filter is adjusted for precise measurement of inductor current; the filter cut-off frequency 1/RC becomes equal to the inductor bandwidth R_{ESR}/L (i.e., from Equations 6.16, 6.17, and 6.18), and current-sensing gain α is set to

$$\alpha = \frac{V_{Cal}}{KI_{DC}}. \tag{6.17}$$

After calibration phase is finished, the switching regulator resumes its normal operation and the g_m-C filter measures the inductor current accurately (i.e., $V_{Sense}=\alpha I_L$).

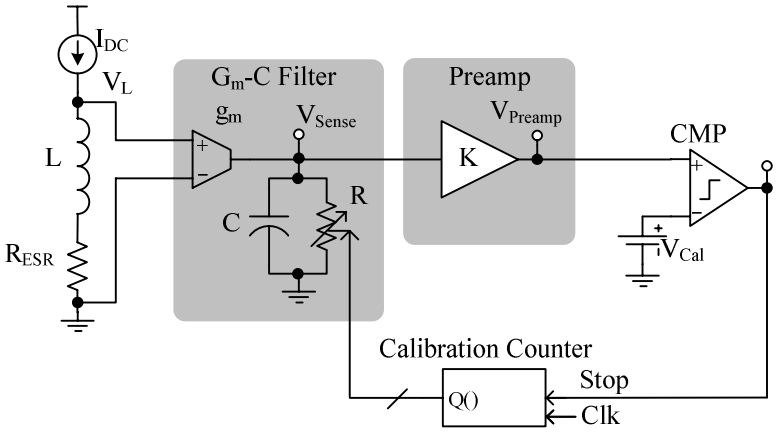


Figure 6.25— Basic calibration block diagram.

Figure 6.26 shows the detailed circuit implementation of the calibration circuit. The circuit is similar to the tuning circuit and uses identical preamplifier and comparator stages. However, the circuit uses a technique called residual successive memorization (RSM) to reach low offset levels as low as few microvolts [90]. The idea is to divide the gain stage into multiple stages with relatively low gain (<20) and compensate for the offset in several locations. At the time of compensation, the gain stages are sequentially auto-zeroed and compensated for from input to output. Therefore, the system compensates for offset-cancellation errors such as clock feed-through and charge injection of the front end at the output stage without saturating the output, and therefore lower offset errors can be achieved by using small hold-capacitors. In addition to SW1, SW2, φ1, and φ1n clocks in tuning, φ2, φ2n, and C_CLK clocks are added to control multi-phase offset-cancellation in calibration.

In the first phase, SW1, φ1, and φ2 are "1" and SW2, φ1n, and φ2n are "0" and the g_m-C filter and comparator are measuring their offsets. In the second phase, φ1 becomes "0" and φ1n becomes "1" while the other clock signals maintain their value. As a result, the g_m-C filter is in placed in the signal path while its inputs are still connected together and AZ_CMP is still measuring its offset at capacitor C_{h22}. However, clock feed-through and charge-injection errors caused by opening φ1 are measured and stored at capacitor C_{h21} at the output of the preamplifier. In the third phase of operation, SW1 and φ2 become "0" and SW2 and φ2n become "1", and consequently filter input connects to inductor ports and AZ_CMP is placed in signal path. The overall offset is very small since errors such as charge injection and clock feedthrough from switches φ1 and φ1n of g_m-C filter are stored in capacitor C_{h21} and are compensated in the second phase. The output of comparator is sampled in the middle of third phase at the rising edge of *C_CLK*. As a result, *Cal_stop* triggers from "0" to "1" if the g_m-C filter has acquired enough DC gain. If the filter DC gain is not large enough, the gain is increased at the next rising edge of SW1 by increasing resistor R. The calibration operation continues until Cal_stop is enabled or the calibration counter reaches its lowest count.

The principles behind the RSM technique are illustrated in Figure 6.27. To achieve very low offset levels in auto-zeroing, the charge-injection and clock feed-through errors of switches should be minimized. Measuring and storing offsets at the output of an amplifier instead of at its inputs can greatly reduce these errors since the offset errors are divided by the gain of amplifier. For example, for an amplifier of gain of 10, if an input-stored auto-zeroing scheme is used, a 100 μV charge injection and clock-feedthrough errors of switches connecting holding capacitors cause a 100 μV input-referred offset. However, if an output-stored auto-zeroing scheme is used, the input-referred offset is 10 μV. Nevertheless, the output-stored autozeroing schemes are not applicable to high-gain amplifiers (e.g., >20) since the initial value of offset in the offset measuring phase can saturate their outputs. The RSM scheme suggests a solution to applying the output-stored technique to a high-gain amplifier by dividing the gain of the high-gain amplifier into multiple relatively low-gain stages (<20) and distributing offset-cancellation across these low-gain stages.

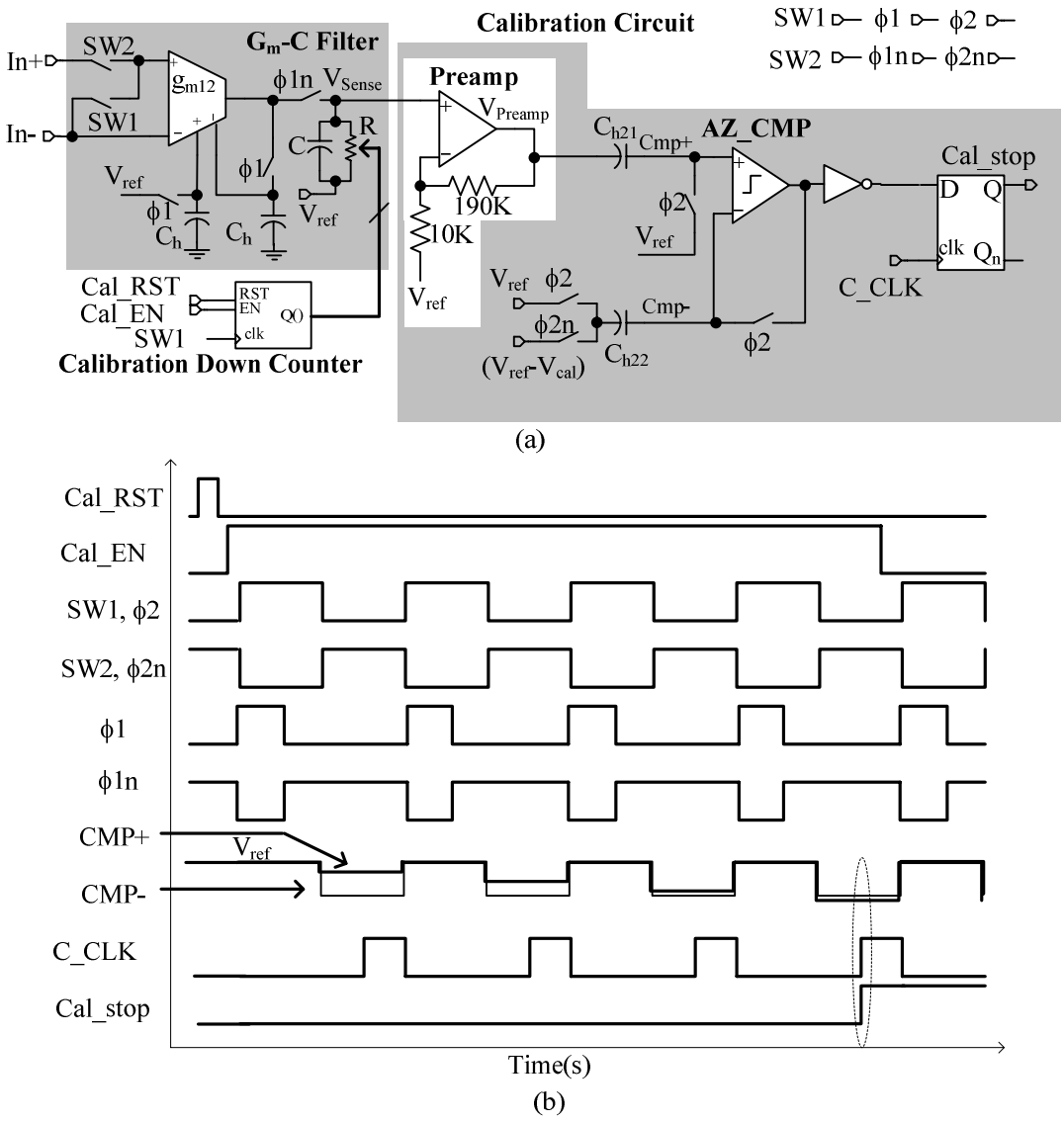


Figure 6.26— Calibration circuit: (a) implementation and (b) waveforms.

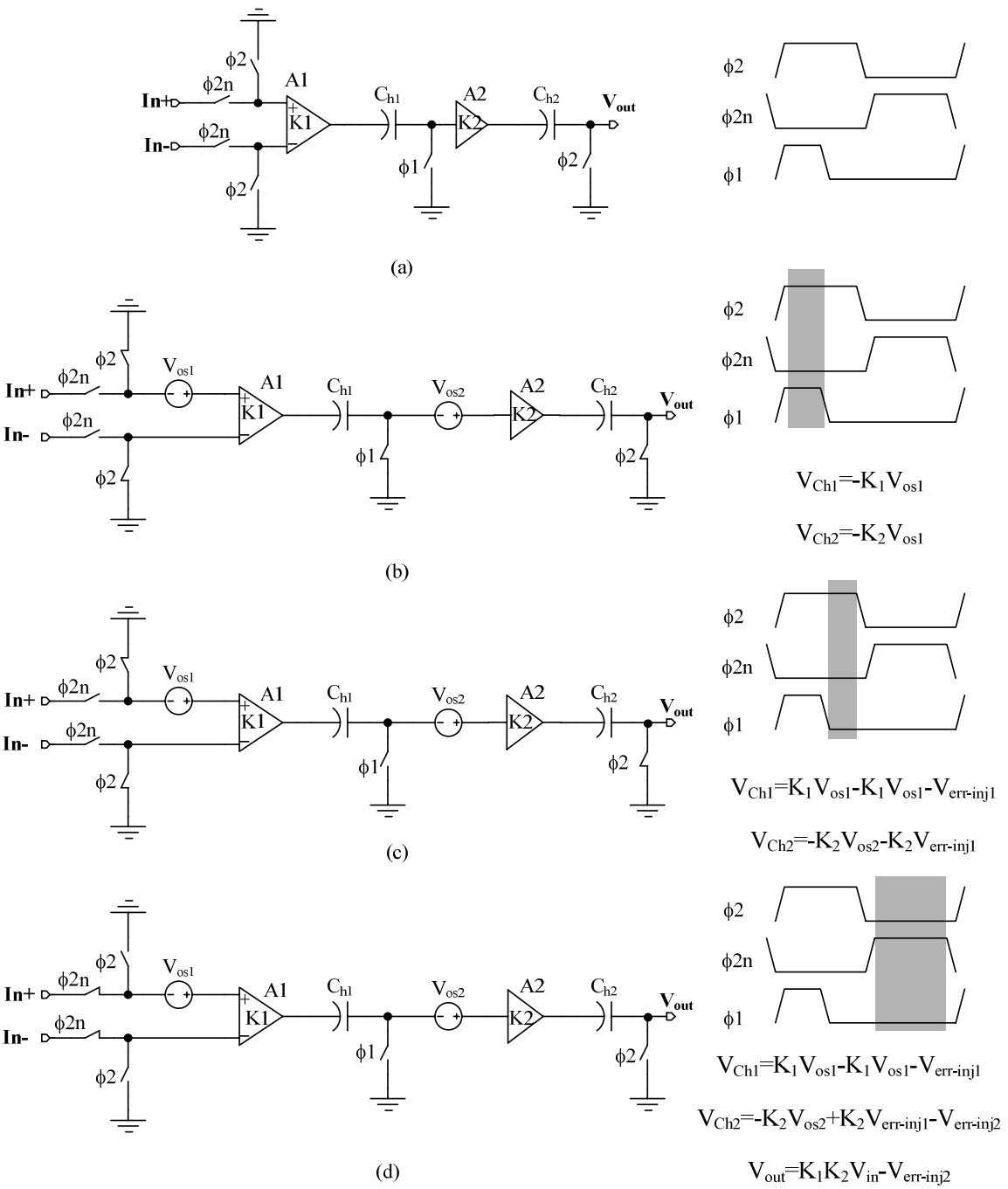


Figure 6.27— Residual successive memorization (RSM) technique to achieve very low-offset levels: (a) schematic, (b) phase1: both amplifiers measure their offsets at their outputs, (b) phase 2: first stage offset-cancellation is disabled but second stage is still offset-canceling and compensates for first stage switch (φ1) clock-feedthrough and charg- injection errors, and (c) phase 3: very-low-offset operation is achieved during normal operation phase.

In Figure 6.27, in phase 1, both amplifiers measure their offset, in phase 2, first-stage offset-cancellation is disabled but the second stage is still offset canceling and compensates for the clock-feedthrough and charge-injection errors of first-stage amplifier switches, in phase 3, very-low-offset operation is achieved in amplification operation since the errors are due to charge injection of the switch φ2 at the output of amplifier. The first phase is necessary to compensate for the first-stage offset and avoid saturation of the second-stage amplifier output in the second phase, where the whole amplifier offset is cancelled at the output.

Figure 6.28 shows details of the proposed calibration loop in three phases of its operation. V135b is the buffered version of V135, which is the 1.35 V reference voltage used in the g_m-C filter as the virtual ground. The overall amplifier in calibration consists of the g_m-C filter as the first stage and the preamplifier as second stage. The hold capacitors C_{h11} and C_{h12} in the g_m-C filter measure and cancel its offset and capacitors C_{h21} and C_{h21} measure and compensate for preamplifier offset, calibration comparator, AZ-CMP offset, and clock-feedthrough and charge-injection errors of switches φ1 and φ1n in the filter .

To speed up the calibration process, the large-output filter capacitor C (60 pF), was removed from the calibration loop using a series switch to reduce the filter settling time. However, this proved to be problematic; the filter noise is increased significantly because the filter bandwidth is increased. The noise is mostly caused by output stage of transconductance g_m because relatively high bias currents are used in transconductance g_m current sources and mirrors, intended to increase the transconductance linearity.

Figure 6.29 shows sampled and averaged voltages at the preamplifier output for minimum and maximum filter resistance R. As resistor R increases, the noise at the filter output increases as well. However, averaging 100 waveforms results in a stable waveform, which proves the noise can be greatly diminished if the filter capacitor C is connected during calibration. To estimate the noise when capacitor C is connected, first the parasitic capacitor at the filter output was determined by bandwidth measurement and its value was found to be 1.33 pF. Then, the peak-to-peak value of preamplifier output voltage with noise was measured, as shown in Figure 6.29(b) (500 mV). This value is approximately equal to four times the output-referred equivalent noise (4σ) [91].

Therefore, the input-referred equivalent noise at input is 500mV/4/20/9.92=0.63 mV, and this is for a 1.33 pF parasitic output capacitor. Consequently, for a 60 pF output capacitor, the input-referred equivalent noise is reduced to 0.63 mV·$(1.33/60)^{0.5}$ = 93 μV.

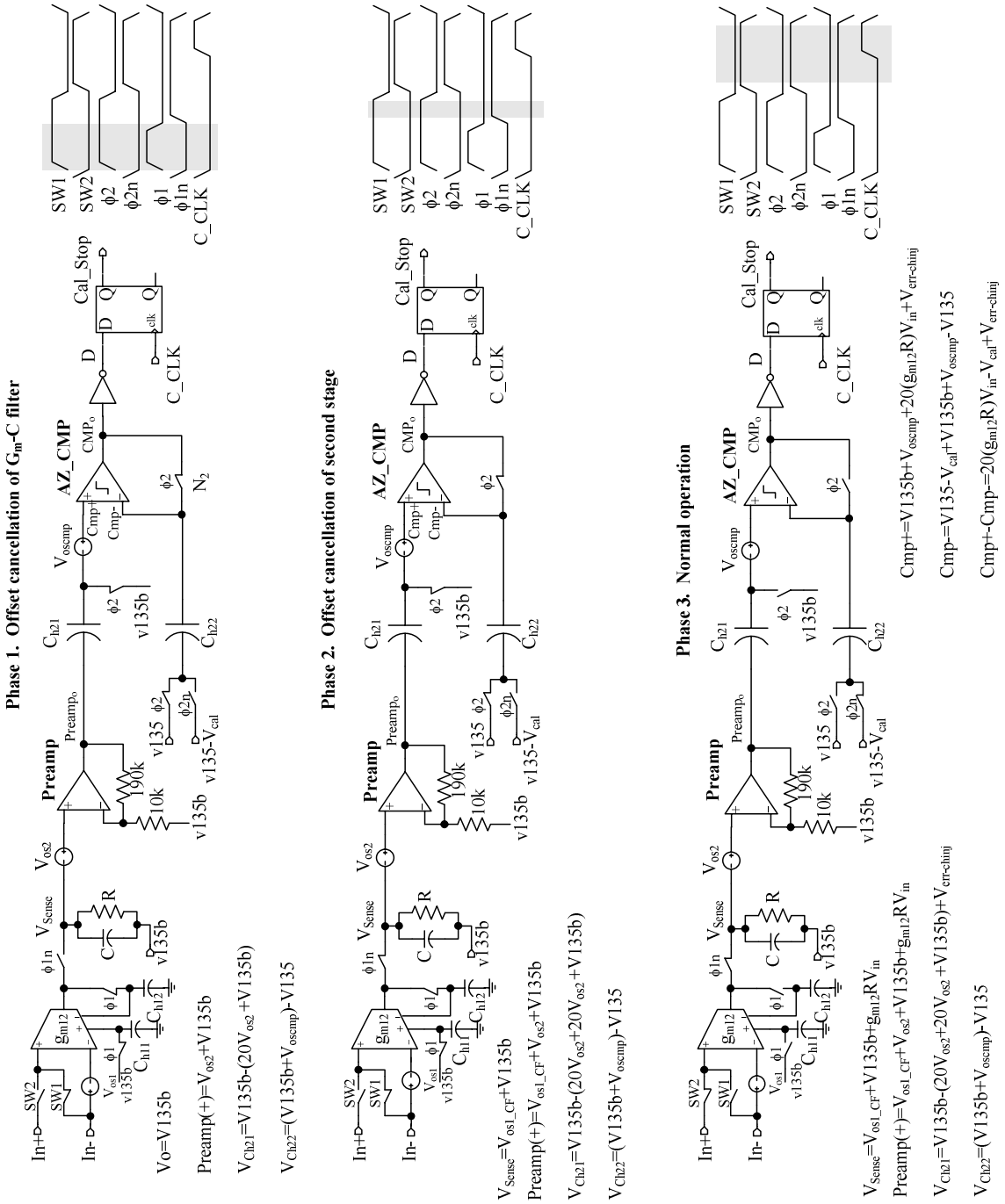
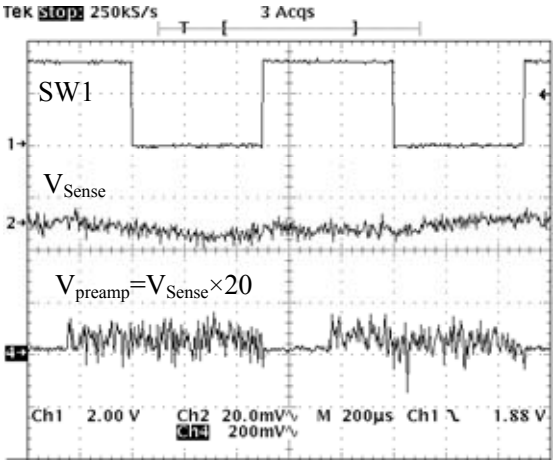


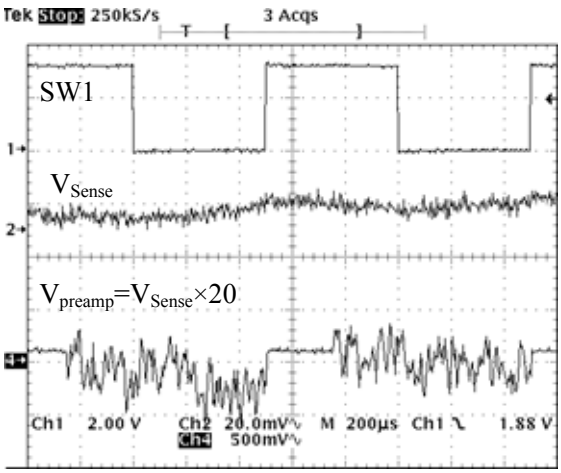
Figure 6.28— Illustration of offset-cancellation mechanism in proposed calibration loop.

V_{indif}=0 V, V_{DD}=3 V, V_{incm}=1.2 V
g_m=min R=min



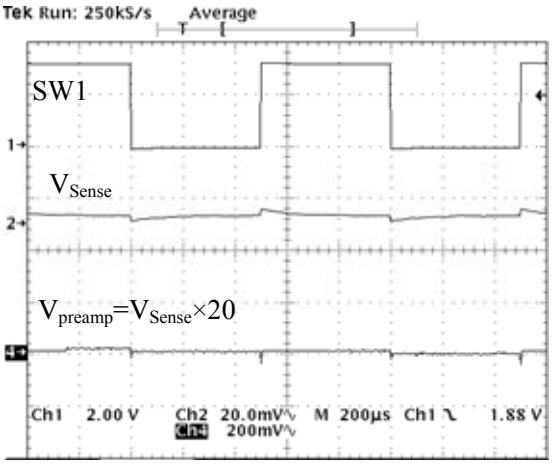
(a)

V_{indif}=0 V, V_{DD}=3.2 V, V_{incm}=1.2 V
g_m=min , R=max, g_mR=10



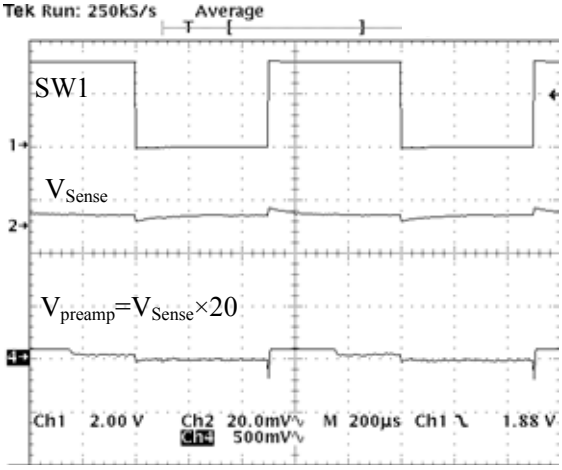
(b)

V_{indif}=0 V, V_{DD}=3 V, V_{incm}=1.2 V
g_m=min R=min



(c)

V_{indif}=0 V, V_{DD}=3 V, V_{incm}=1.2 V
g_m=min , R=max, g_mR=10



(d)

Figure 6.29— Filter and preamplifier outputs at calibration (C=1.33 pF): (a) sampled for g_mR=1.27 (b) sampled for g_mR=10, (c) averaged for g_mR=1.27, and (d) averaged for g_mR=10.

Figure 6.30 shows the averaged (100 waveforms) filter and preamplifier outputs in calibration loop for 0 mV and 2.2 mV output. Because of the noise issue, there is an error in the calibration loop operation since the Cal_stop is triggered sooner than expected and DC gain is set up with about -25% of error. To verify the problem and characterize the calibration loop, the output of the calibration loop Cal_stop was disconnected from the digital core and an additional off-chip circuitry was placed

between the calibration-loop Cal_stop output and the digital core Cal_stop input (Figure 6.31). The off-chip circuit is a comparator that compares the DC value of internal comparator V_{Comp} with half of supply rail (i.e., $V_{DD}/2$). If there were no noise, the internal comparator output would be either zero or one, but because of inherent noise, when V_{amp} becomes close to V_{Cal}, its output is a stream of zero and ones, but its average can be used to measure the offset-cancellation performance of the calibration loop. Since the noise is random, when the loop settles at the target gain (i.e., $(g_mR).20.R_{ESR}I_{Test} = V_{Cal}$) internal compotator DC output is at half of the rail, $V_{DD}/2$. Therefore, an external comparator is used to compare the internal comparator output with $V_{DD}/2$ and control the calibration counter.

To measure the calibration offset, the calibration loop was run for a known input voltage, V_{in}, until the loop was locked (i.e., the calibration loop has stopped) and the calibration gain, at the locked position was measured (i.e., g_mR). Consequently, the input-referred offset of the loop can be determined as

$$V_{off} = \frac{(20(g_mR)V_{in}) - V_{Cal}}{20(g_mR)}, \qquad (6.18)$$

where V_{Cal} is the target calibration voltage (0.5 V) and V_{in} is the DC voltage at the inputs of the g_m-C filter during calibration. The measurement can also be performed open loop, with setting the filter gain and changing the input voltage until the average output voltage of internal comparator becomes $V_{DD}/2$, and then using Equation 6.18 to estimate the input-referred offset. The small increments of input voltage can be obtained by using resistor dividers. The input-referred offsets measured for various gains using the aforementioned method are illustrated in Figure 6.32. The minimum offset is 76 μV at the gain of 6.66. The input-referred offset is higher at low gains since the charge-injection and clock-feedthrough errors at the output are attenuated with low gains at the input. The input-referred offset increases at higher gains since the magnitude of amplified noise at the preamplifier output becomes so large that the preamplifier output is partly clamped. Therefore, the averaging of the capacitor output does not compensate for random offset anymore. It is expected that better offset performance is achieved once the filter capacitor is connected during calibration. The calibration circuit performance is summarized in Table 6.7.

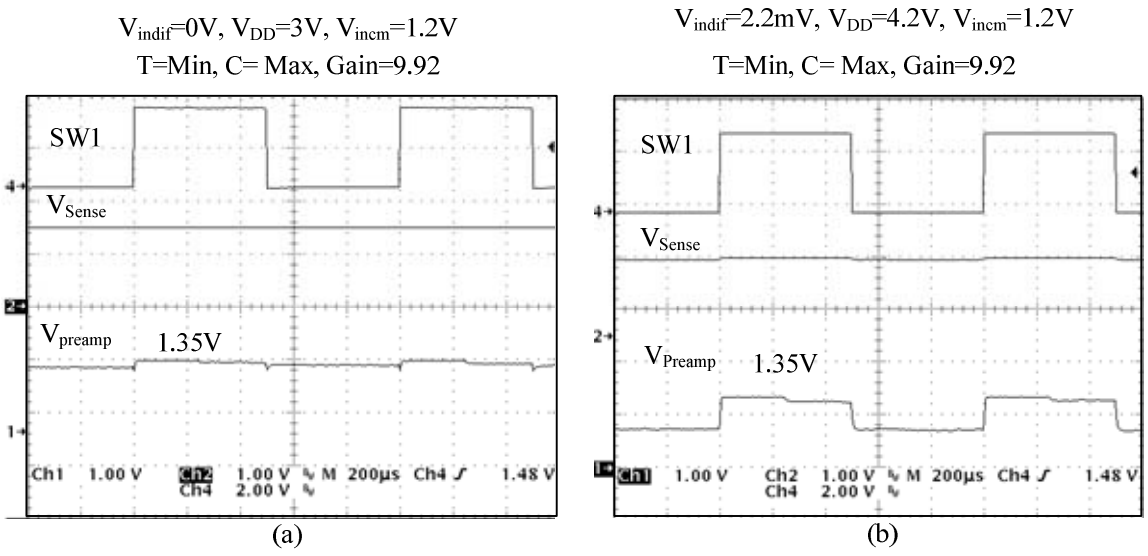


Figure 6.30— Filter (V_{Sense}) and preamplifier ($V_{Preamplifier}$) averaged outputs in a calibration loop (a)V_{in} = 0, g_mR = 9.92 and (b) V_{in} = 2.2 mV, g_mR = 9.92.

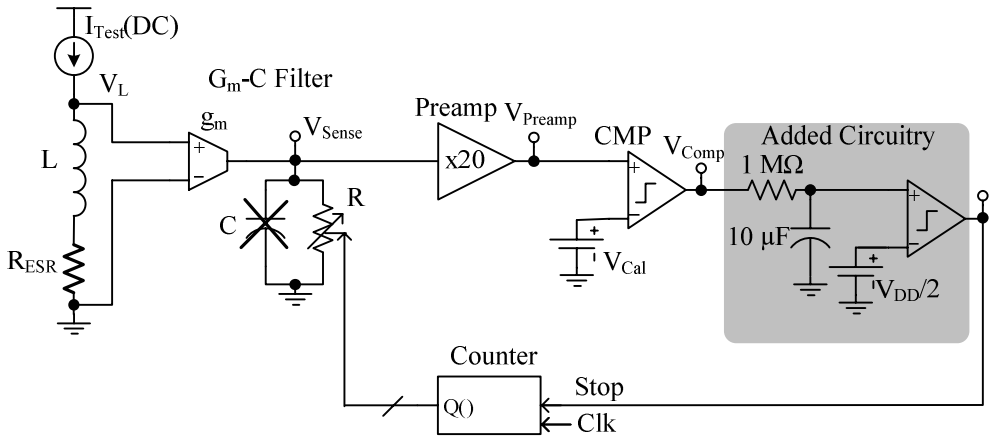


Figure 6.31— Disconnecting output filter capacitor at the calibration phase increases its bandwidth and noise and reduces the calibration accuracy. An off-chip filter and comparator are used to bypass the problem.

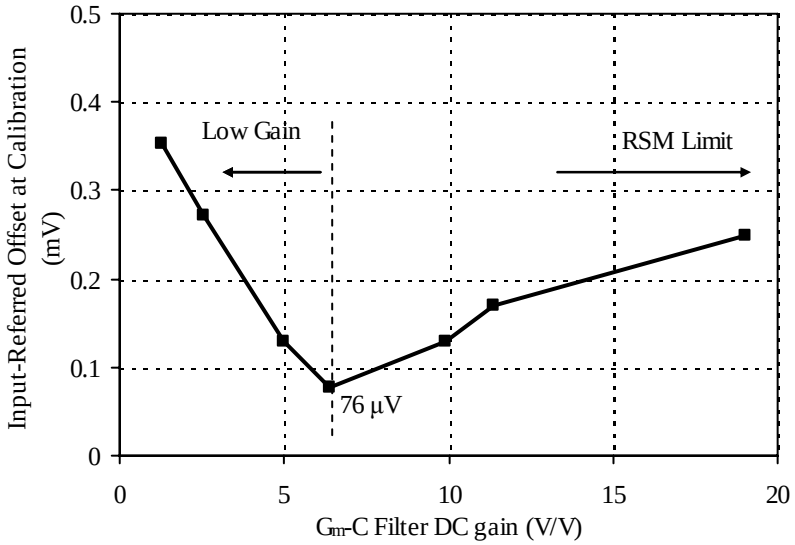


Figure 6.32— Calibration loop input-referred offset versus filter DC gain.

Table 6.7— Specification compliance matrix for the calibration loop.

Spec. Comp.	Target	Sim.	Expr.	Notes
Calibration Loop DC Gain Target	0.5 A/V	0.5 A/V	0.5 A/V	
Total Error	<±3.125%	<±3.125%	<5.4%	R_{ESR}>48 mΩ
Test Current I_{test} (DC)	50 mA	50 mA	50 mA	DC current
Power Supply (V_{DD})	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V - 4.2 V	Calibration-only chip
Error Budget Details				
Preamplifier Gain Error	<±0.5%	±0.11%	-0.23% ±0.125%	DC gain, based on five samples
Offset Error	<±1%	<±1%	<±5.4%	R_{ESR}>48 mΩ
V_{ref} + AZ Offset Errors	<±0.5%	<±0.5%	NA	
I_t error (R_{ref})	<±1%	<±1%	<±1%	
Quantization error	<±1.5%	<±0.75%	NA	For typical value of filter R
Total error	<±3.125%	<±3.125%	< 8%	Experimental results include filter random and systematic offset in normal operation

6.2.4. Tuning/Calibration/G_m-C Filter Clock Generator

This unit is responsible for providing appropriate clock signals to g_m-C filter (during normal operation, turning, and calibration), to tuning loop (during tuning), and to calibration circuit (during calibration). The schematic of the clock generator is shown in Figure 6.33. The circuit input, *PulseIn*, is a 4-kHz clock input from the wave-generator block and its outputs are SW1, SW2, φ1, φ1n, φ2, φ2n, C_Clk, and C_Clkn. The control signal, CalENn from the digital core, determines whether the circuit is generating clocks for calibration or tuning/normal operation modes. Implementation of non-inverting clock generators, which are required to prevent cross wiring, is shown in Figure 6.34. The output waveforms for are illustrated in Figure 6.35.

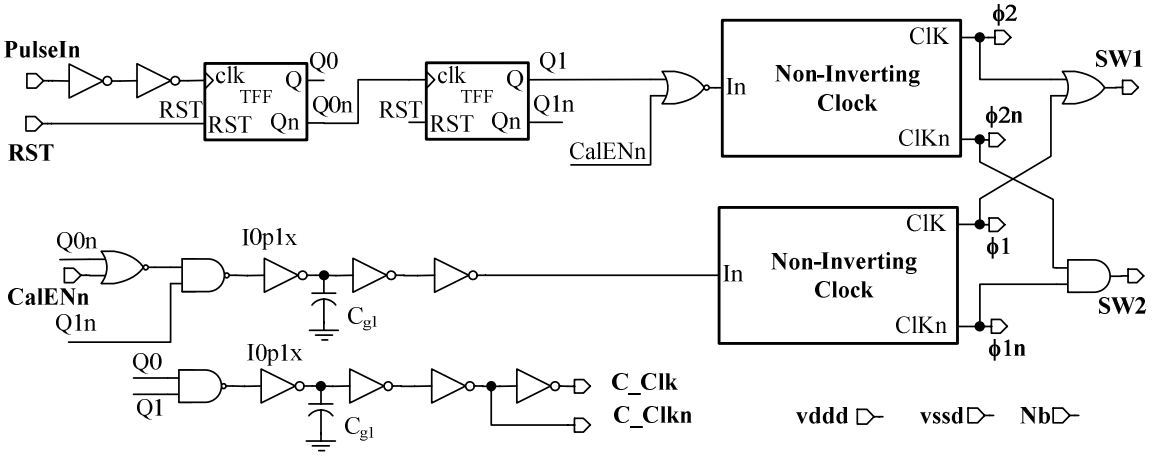


Figure 6.33— Tuning/calibration/g_m-C filter auto-zeroing clock generator schematic.

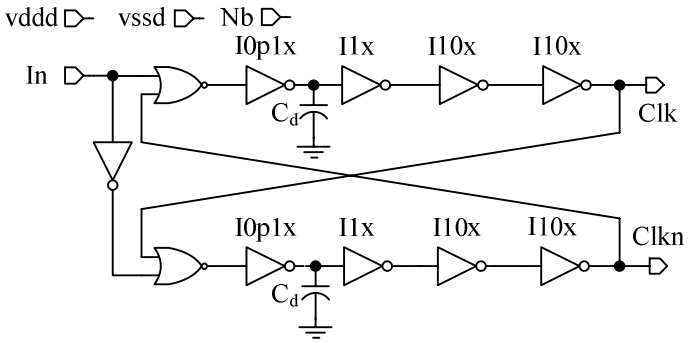


Figure 6.34— Non-inverting clock generator schematic.

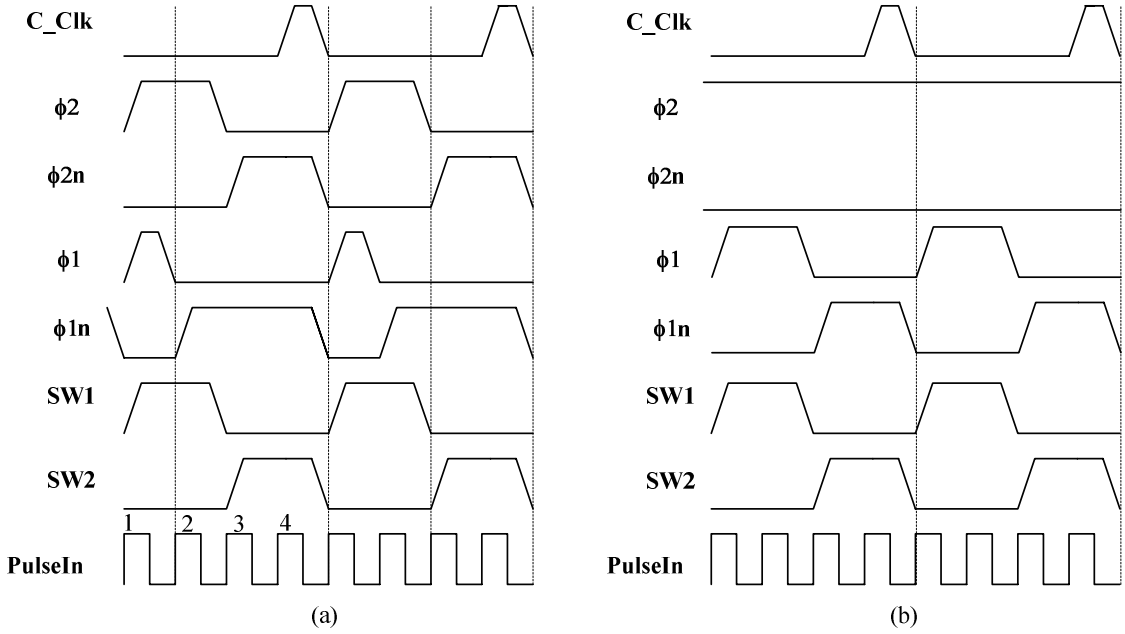
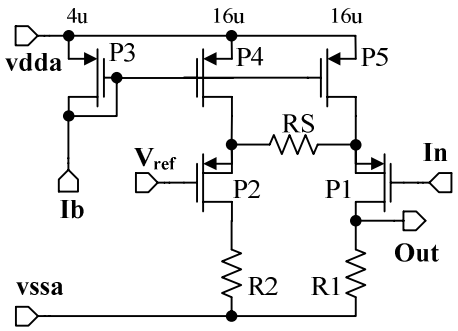


Figure 6.35— Auto-zeroing clock generator output waveforms for (a) calibration phase and (b) tuning/normal operation phases.

6.2.5. Current-Sensing Output Inverter

Since its topology causes the output of the g_m-C filter to be inverted, the output should be inverted once again before it is interfaced to the current-mode controller. Therefore, this analog inverter block is designed to connect the output of g_m-C filter (i.e., current-sensing filter) to the sensed-current input of current-mode controller and its schematic is illustrated in Figure 6.36. The input V_{ref} is the same virtual ground level used in the g_m-C filter for bidirectional operation. Because of relatively low loop gain in this circuit, its gain changes slightly with input voltage level and temperature, however the change is a non-issue since the current-mode controller is not as sensitive to the gain variations of current sensor as it is to its noise and delay (i.e., for current-mode controllers, precise but not necessarily accurate current-sensing is required).



P1	P2	P3	P4	P5	RS	R1	R2
4(10/2)	4(10/2)	2(12/4)	8(12/4)	8(12/4)	40k	20k	20k

Figure 6.36—Current-sensing output inverter.

6.2.6. Test-Current Generator

The test-current generator block, shown in Figure 6.37(a), converts the test signal from voltage to current and forces it into the inductor during start-up (i.e., tuning and calibration). The input voltage V_{in}, which is referenced to the supply voltage and comes from the reference during calibration and from wave generator during tuning, is forced across the test resistor R_t through a negative feedback loop formed by amplifier A_{TCG} (GBW = 10 MHz) and transistor M_a. Therefore, a test current given by V_{in}/R_T flows into the transistor M_a and regulator's switching node (V_{ph}). At start-up where both power switches M_H and M_L are turned off by the driver and DTC unit, the test current flows exclusively into the inductor (Figure 6.37(b)). During tuning, the triangular output of the wave generator is connected to V_{Test}, which forces a triangular current into the inductor and at calibration a DC voltage, referenced to supply, causes a DC current to flow into the inductor. Since triangular current contains high-frequency components, it causes oscillation at the phase node because of an LC tank formed by inductor L and power-switch parasitic capacitor C_{Par} (Figure 6.38(a)).

To damp these oscillations, a damping resistor R_{damp} (about 200Ω) is placed across the inductor at the start-up (Figures 6.37(b) and Figure 6.38(b)), which is large enough to let most of the test current (>99%) to flow into the inductor. The resistor R_b sets the DC value of converter output voltage V_o during start-up to R_bI_{Test}(DC), which is higher than minimum common mode range of the g_m-C filter negative input port and lower than the load turn-on limit. The complete circuit for the test-current generator block

is shown in Figure 6.39. Depending on the start-up state, which is acknowledged to the block by *Tune_EN* and *Cal_EN* signals from digital core, the constant DC voltage or a triangular voltage is connected to the amplifier input. The unit is disabled during the normal operation by turning off M_a, M_b, M_{damp}, and amplifier A_{TCG}. Resistor R_t is chosen to be external to achieve high accuracy (<1%) for the test current. To achieve the same accuracy for an on-chip resistor, trimming is required.

Figure 6.40 shows the experimental results on the performance of this block where input signal, output V_{Test}, and phase node waveforms of test current generator in tuning mode. Table 6.8 lists the key specification parameters including target specifications, worst-case simulations, and measurement result values, which verifies that the results are in compliance with target specifications.

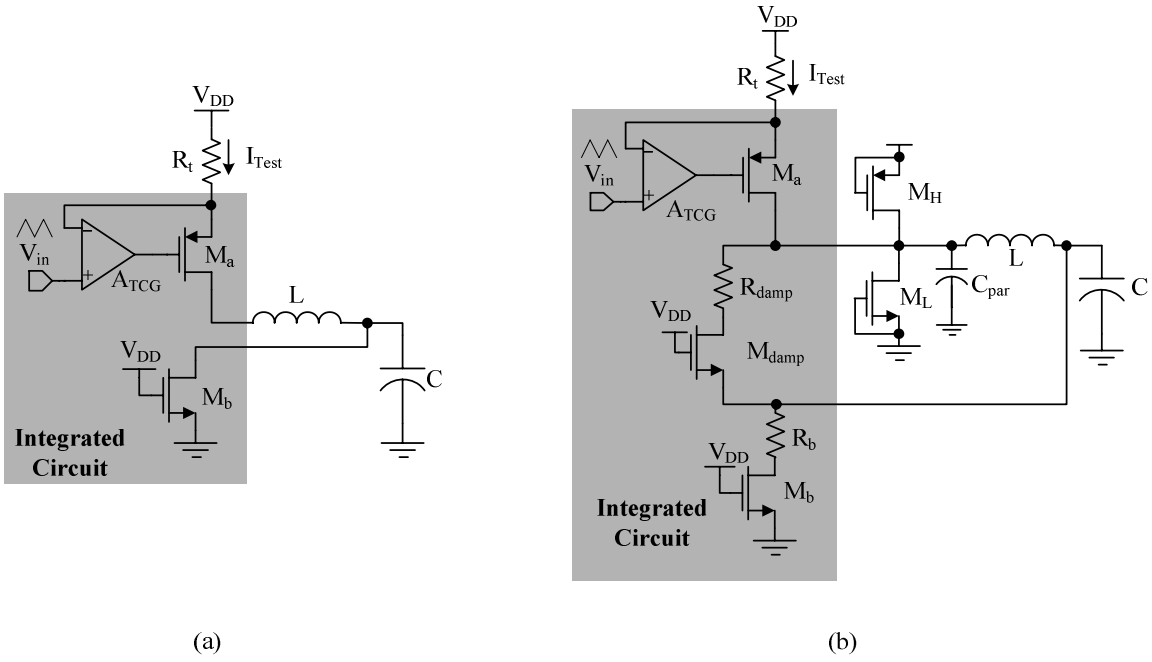


Figure 6.37— Test current generator (a) simple block diagram and (b) with damping resistor to kill oscillations.

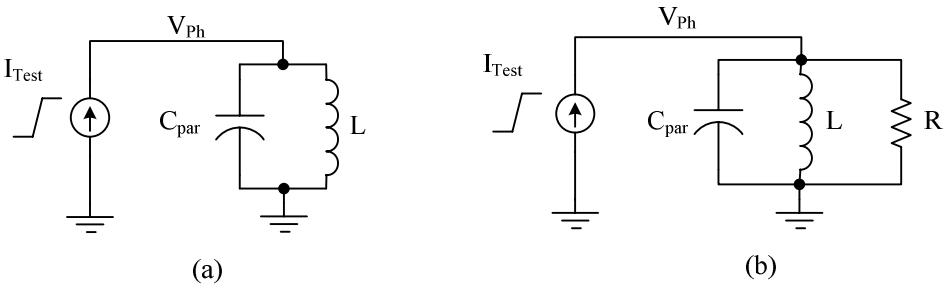
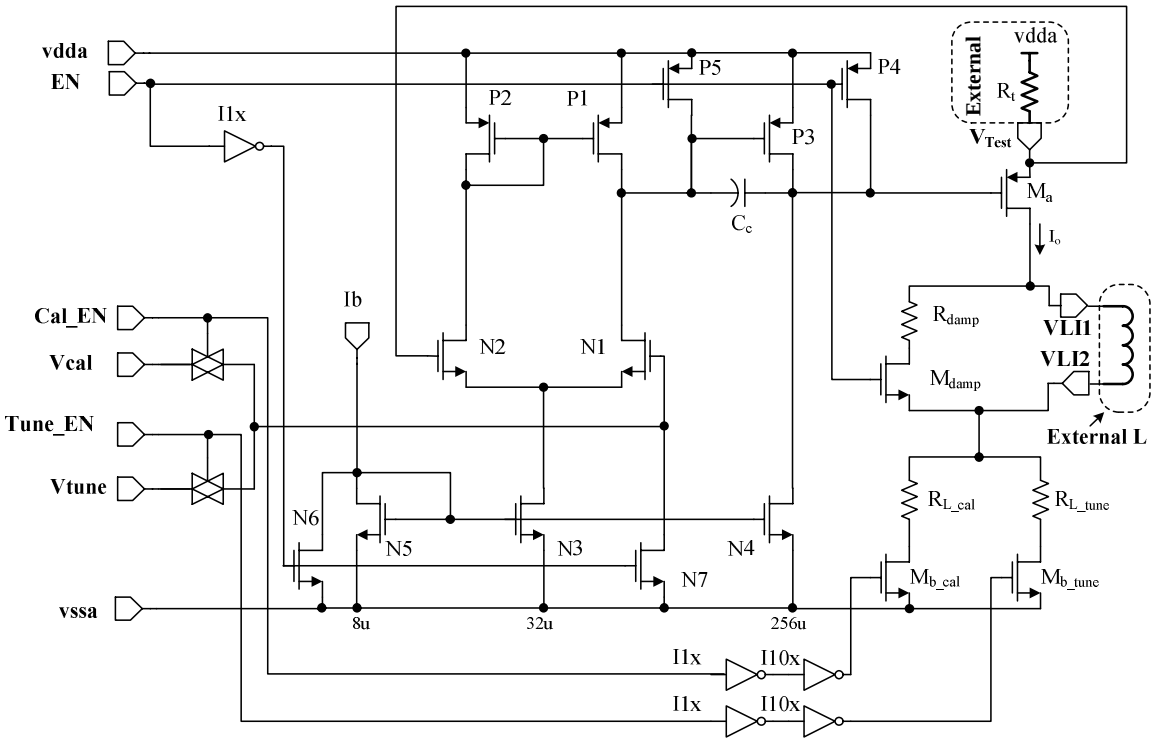


Figure 6.38— (a) A ramp current forced into an LC tank causes oscillation and (b) a damping resistor can kill the oscillations.



R_{damp}	R_{L_cal}	R_{L_tune}	R_t	M_a	M_{b_cal}	M_{b_tune}	C_c
100 Ω	20 Ω	25 Ω	50 Ω	4800/0.6	1200/0.6	1200/0.6	2 pF

Figure 6.39—Complete schematic of the test-current generator block.

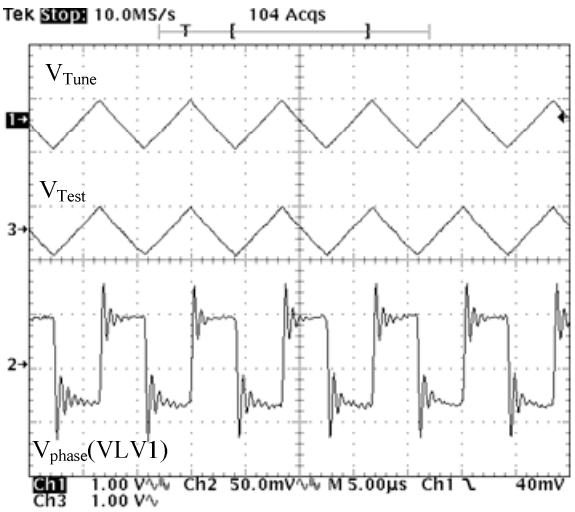


Figure 6.40— Key waveforms of current generator block at tuning, V_{Tune} is the input signal, V_{Test} is the voltage at the test resistor and V_{phase} is the switching port voltage.

Table 6.8— Current generator specification compliance matrix.

Pins and Parameters	Target	WC Sim.	Expr.	Notes
Supply Voltage	2.7 V - 4.2 V	2.7 V- 4.2 V	2.7 V- 3.5 V	
Output Current	DC: 50 mA Tri: 50 mApp	50mA 50mApp	50 mA 50 mApp	
Assigned Error Budget	<±1% (DC) <±2% (AC)	<±1% -1.2%	0% <-1%	DC error function of offset AC error function of BW
R_t Accuracy (external component)	<1%	1%	1%	Target spec from Calibration error budget
ICMR	1.2 - (V_{DD}-0.2 V)	1.6 V - V_{DD}	1.8 V – V_{DD}	Calibration: V_{DD}-1 Tuning : V_{DD}-1.1 to V_{DD}-0.1
Amplifier BW (closed loop, gain=1)	>4 MHz	4.2 MHz	5.77 MHz	<0.2% error for 200 kHz ramp signal
Phase Margin	>72°	50°	>85°	No overshoot at transients
Amplifier A_{TCG} Offset	<2 mV (with trim)	±12 mV (3σ)	NA	For less than 0.2% error
Quiescent Current		50.3 mA 30.3 mA		Start-up, calibration Start-up, tuning

6.2.7. Wave Generator

The wave generator block provides pulse and ramp signals during the normal operation for current-mode controller and provides a triangular signal during start-up for the tuning loop. At tuning, the triangular voltage signal generated by this block is feed to

the test current generator block, where it is converted to a test triangular current forced into the inductor. For high tuning accuracy, the triangular signal should be generated with a tight control on its peak to peak amplitude. The amplitude and frequency of the ramp signal should also be well controlled in PWM controllers. Fortunately, conventional ramp generators used in PWM converters can be slightly modified to generate triangular current. Usually, ramp generator is designed with a very sharp ramp down. This requires very fast, continuous, high power comparators to tightly control the ramp lower level. However, it was found that the very sharp ramp down is not actually required for PWM voltage- and current-mode controllers as it is discussed next.

Figure 6.41 (a) illustrates a representative block-level diagram of a typical voltage-mode PWM DC-DC converter, where V_{Out} is the output of the negative shunt-feedback loop and its value is sensed, amplified, and converted into PWM signal V_{ph} before finally being filtered back into a voltage. The peak-to-peak voltage (V_{in}) and duty-cycle D of V_{ph} determine the value of V_{Out}, which is an averaged version of switching signal V_{ph}. Error amplifier EA modulates D via ramp generator and hysteretic comparator circuits to regulate V_{Out} against reference V_{ref}.

The ramp signal sets the duty-cycle by defining the on-time duration of power switch M_H with comparator PWM CMP. The ramp and on-time start at the onset of the constant frequency pulse (Figure 6.40(b)). The ramp is then compared against the slow-moving output of EA (EA_{out}), and when the ramp surpasses EA_{out}, PWM comparator trips, resets the SR latch, and connects V_{ph} to ground through switch M_L, marking the end of the on-time sequence.

The SR latch ensures only one pair of set-reset events occurs per period. As a result, after a reset, the regulator cannot change state until the onset of the following pulse. The ramp must therefore be linear for the longest worst-case on-time condition, which occurs when duty-cycle D is at its maximum value. D, however, is normally constrained to less than 90% to protect power switch M_H from overheating and exceeding its power-rating limits. Without this protection, D could viably increase to such an extent that M_H is mostly on and conducting exceedingly large current densities. Consequently, the on-time should never exceed 90% of the period, so slightly less than 10% of the

period can be dedicated to reset the ramp (Figure 6.41(b)), which is the motivation for the proposed scheme.

Conventionally to generate ramp signal, after an initial reset event, a capacitor is slowly charged with charge-current I_{Chg} until the capacitor voltage (ramp) reaches upper limit V_H (Figure 6.42(a)), at which point the comparator trips and quickly resets the ramp to ground with low resistance switch S_{Dchg}, marking the beginning of another cycle [92-97]. However, quickly discharging C to ground via a finite-delay comparator causes the lower limit of the ramp to reset below lower threshold V_L, introducing an error equal to

$$V_{Error} = \frac{dV_{Fall}}{dt} t_{Dly}, \tag{6.19}$$

where dV_{Fall}/dt is the capacitor's discharge rate and t_{Dly} is comparator CMP2's delay.

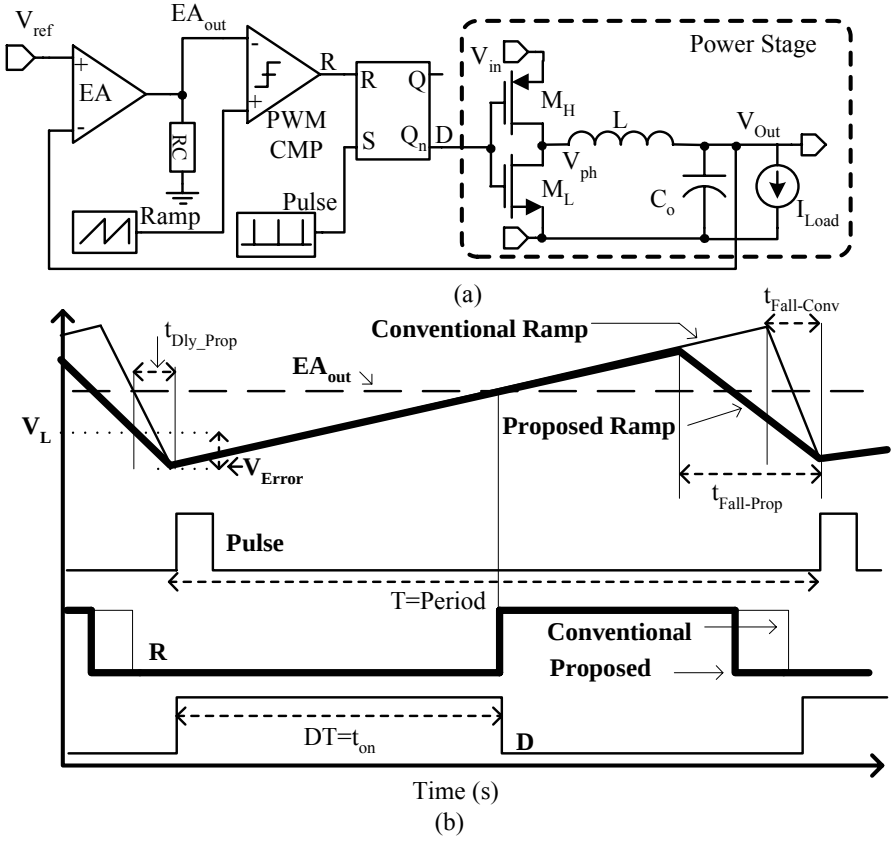


Figure 6.41—(a) Voltage-mode PWM buck converter and (b) respective signals.

Even a few nanoseconds of delay causes an error of hundreds of millivolts because dV_{Fall}/dt is high. The resulting period is therefore the time required to charge C from the less than predictable low voltage peak to V_H,

$$T_{Conv} = \frac{C\left[V_H - \left(V_L - V_{Error}\right)\right]}{I_{Chg}}. \tag{6.20}$$

If a 100 mV peak-to-peak ramp is designed with a 10 V/μs discharge rate, for example, a 2 ns delay comparator is required to limit V_{Error} and the extended period to within 20 mV and 20%.

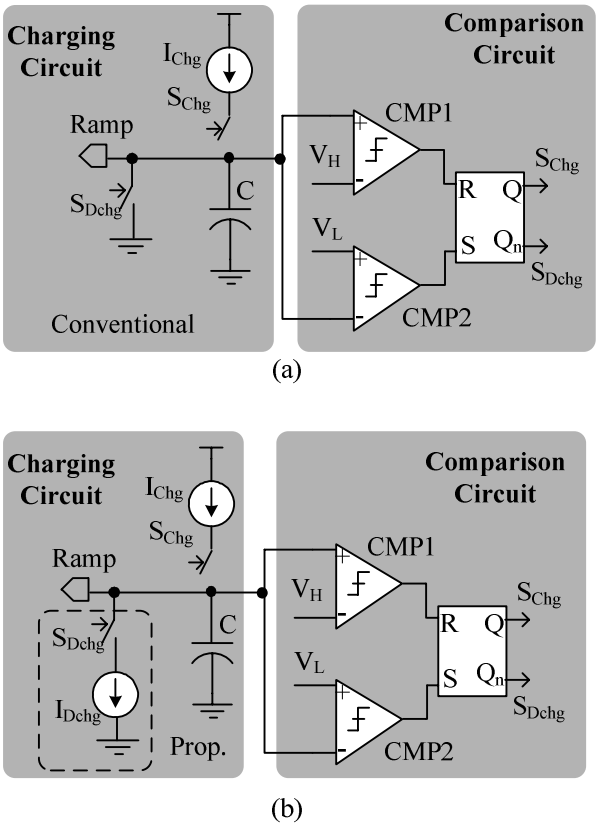


Figure 6.42— (a) Conventional and (b) proposed ramp-generator circuits.

The proposed scheme charges a capacitor with constant charge current I_{Chg} for 90% of the period, until an upper voltage limit is reached, and discharges it with discharge current I_{Dchg} (I_{Dchg}=9I_{Chg}) for the remaining 10%, until the lower limit is surpassed and a new cycle begins. As before, the ramp limits are set with two comparators and the resulting period is

$$T_{Prop} = C\left[V_H - \left(V_L - V_{Error}\right)\right]\left(\frac{1}{I_{Chg}} + \frac{1}{I_{Dchg}}\right). \quad (6.21)$$

Since the negative ramp is now slew-rate limited, the comparator's delay has a lower impact on V_{Error}. For example, if a 100 mV peak-to-peak ramp with a 1 V/µs discharge rate is designed, a 20 ns-delay comparator is required to limit V_{Error} and the period from varying less than 20 mV and 20%; in other words, a 20 ns-comparator in the proposed circuit (Figsures 6.42(b) and 6.43) produces the same results that a 2 ns-comparator does with the conventional approach. Replacing the constant discharge current or switch S_{Dchg} with a high-resistance switch performs a similar function, but the uncorrelated process- and temperature-dependence of the resistor introduces uncertainty in the discharge cycle and consequently frequency and the 10% duty-cycle region.

In the proposed circuit of Figure 6.43, bias current I_b and mirrors N0,1,2 and P1,2 set the charge- and discharge-current ratios (Figure 6.43(a)). Switches N4 and P4 reduce transient on-off mirror glitches by preventing transistors N2 and P2 from turning off when they are disconnected from C. For speed, the comparator is comprised of two low gain, high BW, resistively loaded stages; a high gain, high swing stage; and three digital CMOS inverters (Figure 6.43(b)) [89].

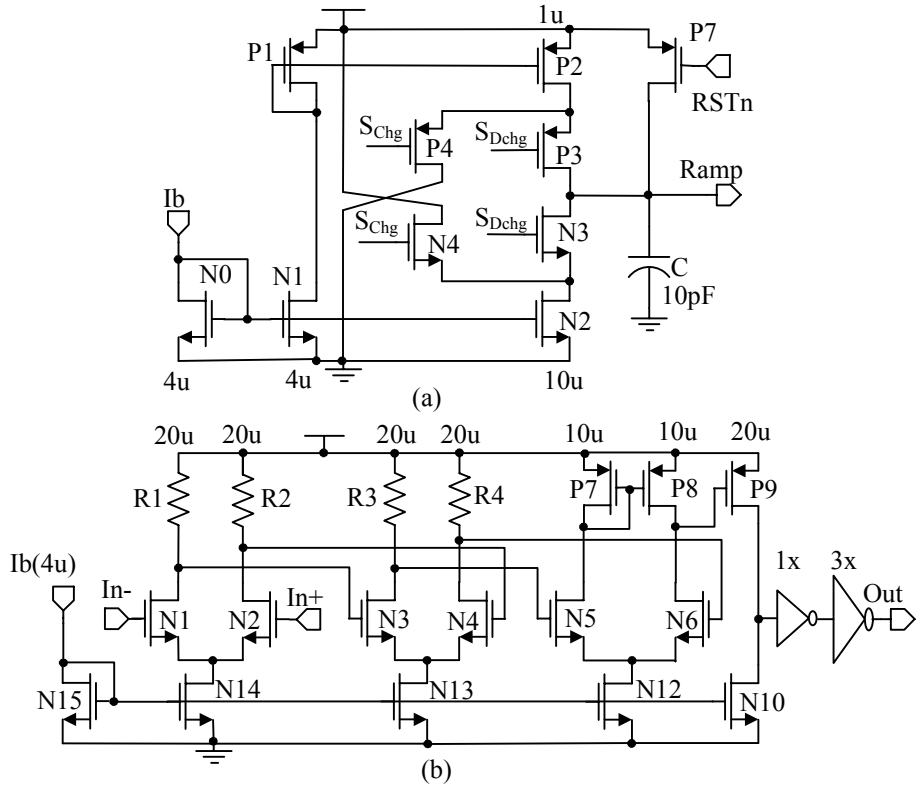


Figure 6.43—Proposed 0.5-µm CMOS (a) charger/discharger and (b) comparator.

For the same rising ramp-rate and frequency (Table 6.9), as required by a PWM DC-DC regulator, the proposed ramp generator requires much slower comparators than conventional schemes (20 ns versus 2 ns). The cost is limited duty-cycle range (D≤90%), but regulators are usually prevented from reaching these limits anyway, to protect the switches from overheating and exceeding power-rating limits. More importantly, the resulting power and silicon area savings from relaxing the performance of the comparator is crucial in portable electronics where light-loading power losses limit battery life.

Table 6.9— Comparison of the proposed and conventional schemes.

	$\frac{dV_{Rise}}{dt}$	$\frac{dV_{Fall}}{dt}$	t_{Fall}	t_{Rise}	D_{Max}	V_{Error}	t_{Cmp_Dly}
Conventional	0.1 V/µs	10 V/µs	0.01 µs	1 µs	99%	20 mV	2 ns
Proposed	0.1 V/µs	1 V/µs	0.1 µs	0.9 µs	91%	20 mV	20 ns

The complete wave generator circuit is illustrated in Figure 6.44. Depending on the value of Tune_EN control signal from the digital core, the circuit generates either

ramp or triangular signal. An 8-bit counter is added to derive a low frequency, 4 kHz, clock from the output of the SR latch (S_{Dchg}). This signal is used as the input clock to the calibration/tuning/filter clock generator block (Section 6.2.5). The 256 µA ramp generator (charger/discharger and two 32ns-delay comparators) operates with supply voltages as low as 1.8V. For ramp, the high and low ramp limits are 1.4 V and 1.3 V and operation frequency is 800 kHz. For triangular signal, these limits are at V_{DD}-0.2V and V_{DD}-1.2V, and 100 kHz where V_{DD} is the supply voltage.

The specification compliance matrix in Table 6.10 summarizes the simulation and experimental results for this block. Experimental waveforms of the outputs of this block are illustrated in Figure 6.45. The ramp in Figure 6.44(a) is only 320 kHz because the probe capacitance slowed it down. Without the probe, the ramp had a switching frequency of 769 kHz, as proved by the PWM waveforms. The 12 mV negative peak error of the probed 320 kHz signal extrapolates to a 28 mV peak error for the 769 kHz ramp, which closely agrees with simulations. The triangular signal waveform is shown in Figure 6.44(b), where its peak-to-peak value is 1 V.

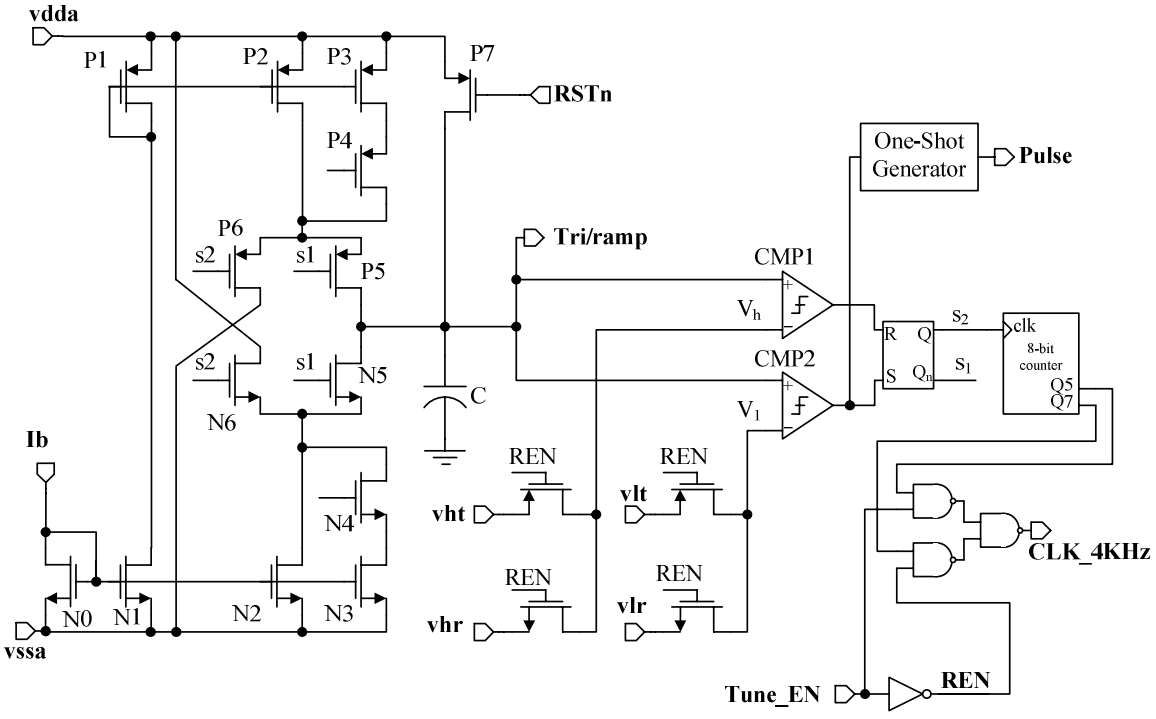


Figure 6.44— Complete schematic of wave generator block.

Table 6.10— Wave generator specification compliance matrix.

Pins and Parameters	Target	Nom. Sim.	Exp.	Notes
Supply Voltage (V_{DD})	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V – 3.5 V	
V_{Hr} (in)	1.4 V	1.4 V	1.4 V	High-voltage limit for ramp
V_{Lr} (in)	1.3 V	1.3 V	1.3 V	Low-voltage limit for ramp
V_{Ht} (in)	V_{DD}-0.2	V_{DD}-0.2	V_{DD}-0.2	High-voltage limit for tri.
V_{Lr} (in)	V_{DD}-1.2	V_{DD}-1.2	V_{DD}-1.2	Low-voltage limit for tri.
Ramp Output Peak to Peak	0.1 V	0.127 V	0.127 V	Based on two samples
Ramp Output Freq.	1 MHz	770 kHz	769 kHz	Based on PWM controller
Triangle Output Peak to Peak	1 V	1 V	1 V	Based on two samples
Triangle Output Mag. Error	<1%	<2.2%	+1.6%	
Triangular Output Freq.	100 kHz	100 kHz	98 kHz	Capacitor probe at its output
Comparator Offset	<5 mV	NA	NA	
Comparator Delay	12.5 ns	20 ns	NA	< 0.5% error at 100 kHz 5 mV input
Quiescent Current		256 μA	NA	

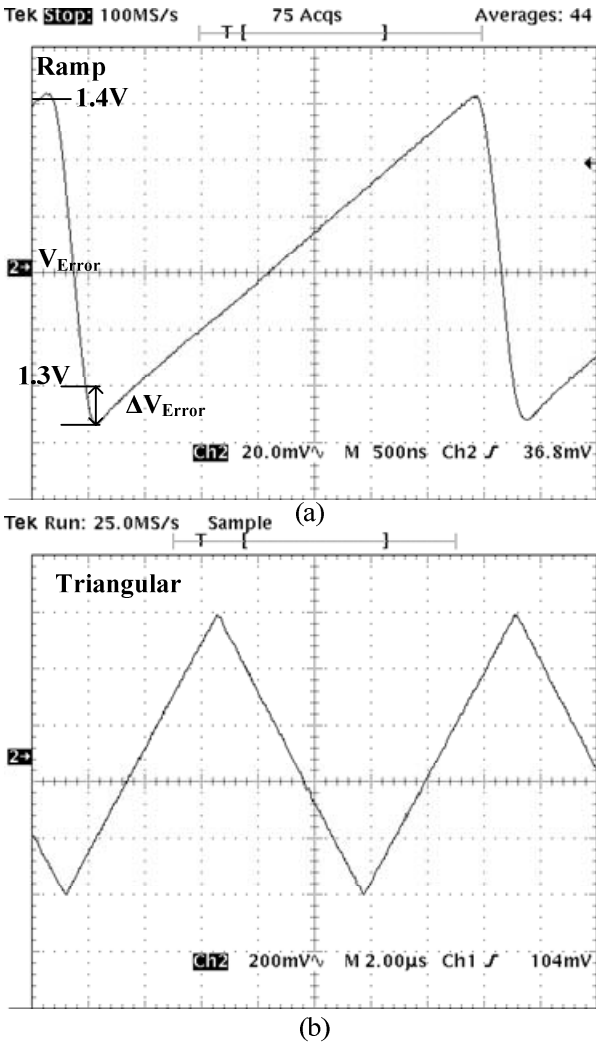


Figure 6.45— Waveform generator output signals: (a) probed ramp signal at calibration and normal operation and (b) triangular signal at tuning.

6.2.8. Current-Mode Controller

To verify the operation of the proposed current-sensing circuit in the system, a PWM current-mode buck converter was devised. The converter was designed for a portable battery-operated Li-Ion battery (i.e., V_{in}=2.7 V - 4.2 V) and a digital processor output (V_o=1.5 V, I_L<1 A) application. The overall system is illustrated in Figure 6.46 and consists of a power stage, a current-sensor, and a current-mode controller that includes driver and dead-time controller, ramp and pulse generator, a summing comparator and an error amplifier as well as housekeeping blocks such as reference and bias network and digital core.

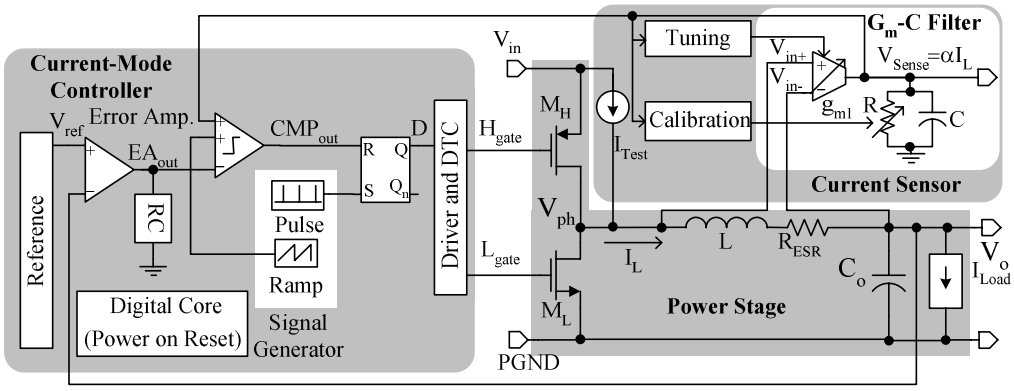


Figure 6.46— Self-learning current sensing circuit applied to a current-mode controller.

The buck regulator converts the supply voltage V_{in} to a lower output V_o without the excessive power losses of linear regulators. The phase node (V_{ph}) is a connected to the input voltage or ground through high-side switch M_H and low-side switch M_L and, therefore, its voltage is a rectangular signal with an average of DV_{in}, where D is the duty cycle of switching (i.e., percentage of the time M_H is on in a switching cycle). A negative shunt feedback through the error amplifier sets regulator's output voltage V_o to reference voltage V_{ref} and feeds the error signal to the current-mode modulator. In a PWM peak current-mode controller, the switching frequency is constant and a switching cycle starts with a periodic pulse setting an RS latch and turning on the high-side switch. Consequently, the inductor current starts ramping up. When the inductor current (converted to voltage at the current-sensing circuit) exceeds the slow-moving error amplifier output EA_{out} the comparator output toggles up, resets the RS latch, turns M_H off and turns M_L on. A ramp signal is usually subtracted from the error amplifier output at the other input port of the summing comparator to reduce noise sensitivity and prevent large signal instability at duty cycles that are more than 50% (See Chapter 5 on sub-harmonic oscillations).

Detailed configuration of the error amplifier compensation network (i.e., resistors R_a, R_b, and R_c, and capacitor C_z) and soft-start circuitry are illustrated in Figure 6.47. Since current-mode topology transforms the regulator transfer function from error amplifier input to buck converter output to a single-pole response [98-99], the controller can be compensated by choosing proper closed-loop gain for error amplifier feedback (i.e., resistors R_a and R_b). Capacitor C_z adds a low frequency pole and changes the

compensator to proportional-integrator (PI). Consequently, the DC gain is increased, and DC errors are reduced. Resistor R_c sets the buck converter output voltage V_o with respect to reference voltage V_{ref} (i.e., $V_o=(1+R_b/R_c)V_{ref}$). Detailed system-level design of current-mode controller was discussed in Chapter 5.

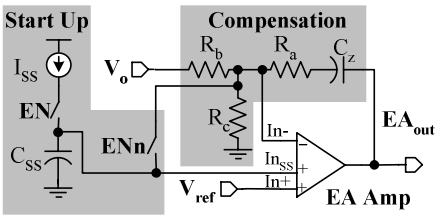


Figure 6.47— Current-mode controller compensation and soft start.

The soft start circuit [100] ensures a slow ramp up of reference voltage and limited in-rush of inductor current. The circuit consists of a current source charging a relatively large capacitor C_{SS} and an error amplifier with a minimum function at its positive input ports, where the lower of two inputs is compared to the negative input. At power-on-reset, the start-up enable signal (EN) is low (Figure 6.47), and therefore the slow start-up capacitor C_{SS} is charged to error amplifier negative input, which is proportional to buck converter output voltage and is lower than its steady-state value V_{ref}. When soft start begins by asserting EN from the digital core, the current-mode controller loop starts working and tries to regulate the output voltage to slow-charging voltage of capacitor C_{SS} through In_{SS} input, which is lower than In+. Eventually, capacitor C_{SS} charges to supply voltage and therefore the loop regulates to In+ input (i.e., V_{ref}). As a result, the positive and negative inputs of error amplifier are kept close together during the soft start, which prevents the error amplifier output from clamping to the positive rail, avoids turning on of the high-side switch for a long time, and prevents excessive inductor current that can damage the power switches. The soft-start circuit was implemented for a 2 ms start-up time, and capacitor C_{SS} is external, as are the passive elements of the compensation network. The top-level implementation of the current-mode controller is illustrated in Figure 6.48 and design of its sub-blocks is discussed in following subsections.

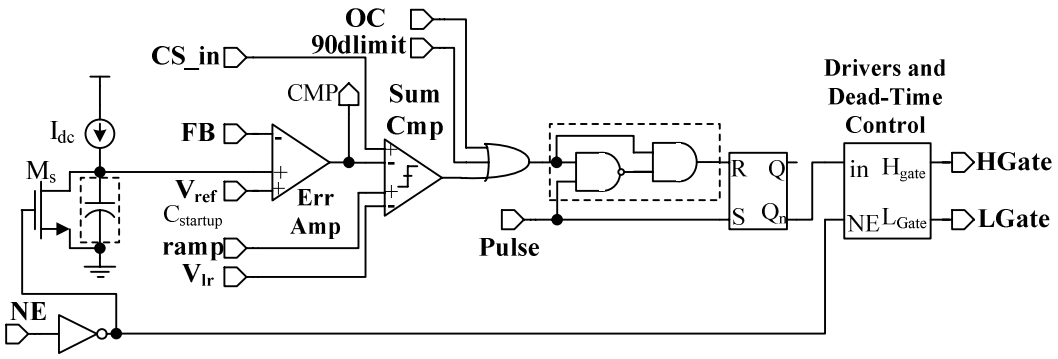
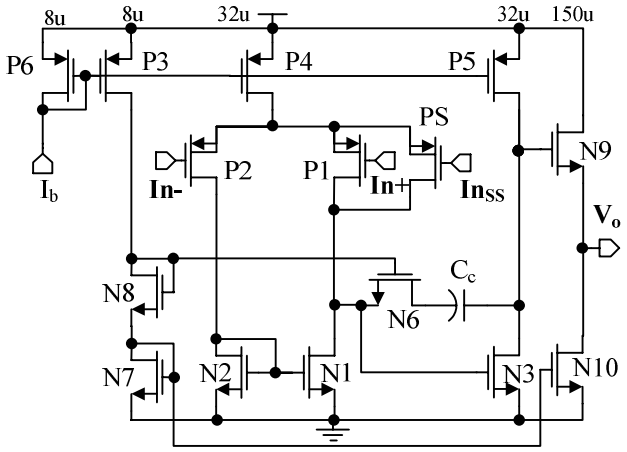


Figure 6.48—Top-level schematic of current-mode controller.

6.2.9. Error Amplifier

A CMOS two-stage amplifier topology [103] was chosen to implement the error amplifier as illustrated in Figure 6.49. The amplifier was designed for a typical 10 MHz bandwidth so that its frequency response does not affect the stability of the current-mode controller, and it uses a relatively high current output stage to drive output pin capacitance of up to 20 pF without degrading stability. Transistor PS, along with transistor P1, generates a "minimum" function at the positive port of the input stage. As a result, the smaller of the two inputs, In_{SS} or In+, constitutes the effective positive input of the differential pair. Simulation and experimental results for this block are summarized in Table 6.11.



P1	P2	PS	P3	P4	P5	P6	N1
4(15/2)	4(15/2)	5(15/2)	2(12/4)	8(12/4)	8(12/4)	2(12/4)	4(5/4)
N2	**N3**	**N6**	**N7**	**N8**	**N9**	**N10**	**C_c**
4(5/4)	8(5/4)	4(5/4)	2(5/4)	2(5/4)	10(6/0.6)	60(5/4)	1.2 pF

Figure 6.49— Error-amplifier circuit.

Table 6.11— Error-amplifier specifications compliance matrix.

Pins and Parameters	Target	WC Sim.	Expr.	Notes
Power Supply	2.7 V – 4.2 V	2.7 V – 4.2 V	2.7 V – 4.2 V	
ICMR in+	0.1 V – 1.5V	0.1 V - (V_{DD}-1.2)	0.1 V - (V_{DD}-1)	Connected to output voltage
ICMR in-	0.1 V - 1 V	0.1V - (V_{DD}-1)	0.1 V- (V_{DD}-1)	Connected to reference voltage
OCMR	0.1 V- 1.5 V	0.1 V - (V_{DD}-0.1)	0.1 V- (V_{DD}-1)	V_{DD}(min)=2.7 V
Quiescent Current	150µA	290 µA	NA	
Bandwidth (1) **Feedback Gain=1** **Feedback Gain=2**	 10 MHz NA	 8 MHz 4 MHz	 NA 5.42 MHz	
Phase Margin **Gain=1, C=10 pF** **Gain=2, C=48 pF** **Gain=20, C=10 pF**	 >45˚ >72˚	 55˚ NA 79˚	 NA 75˚ NA	1 kΩ feedback resistors
Load Drive Capability	20 pF	20 pF	48 pF	Output Pin
DC Gain	>60 dB	78 dB	NA	
Input-Referred Offset	±20 mV	±11 mV (3σ)	NA	

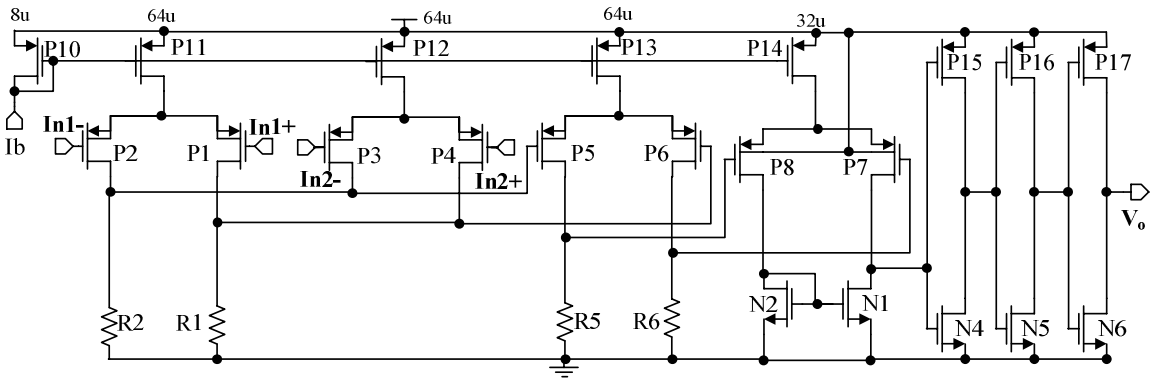
(1) Bandwidth: frequency at which the amplifier gain is reduced to 0.707 magnitude of its low-frequency gain.

6.2.10. Summing Comparator

The circuit implementation of the summing comparator is shown in Figure 6.50 [104]. The circuit is designed for a typical 50 ns delay for a 10 mV overdrive. The first pair inputs, In1+ and In1-, are connected to the current-sensing circuit and the error amplifier outputs, respectively and the second input ports, In2+ and In2-, are connected to the ramp signal generator output and the ramp lower limit (V_{Lr} in Figure 6.44), respectively. The identical differential pairs, P1-P2 and P3-P4, convert input voltages to current and their currents are added to form voltages across resistors R1 and R2. As a result, the differential voltage at the gates of pair P5-P6 becomes

$$V_{56} = g_{m12} R_{12} (V_{In1+} + V_{In2+} - V_{In1-} - V_{In2-}), \qquad (6.20)$$

where g_{m12} is the transconductance of transistors P1-P4 and R_{12} is the value of resistors R1 and R2 in Figure 6.50. Then, the V_{56} difference is amplified by a two-stage amplifier followed by three inverters. Thus, the comparator output triggers a positive supply if the sum of positive inputs is more than the negative inputs. Otherwise, the comparators rails to negative supply rail. Simulation and experimental results for this block are summarized in Table 6.12.



P1	P2	P3	P4	R1	R2	P5	P6
4(15/2)	4(15/2)	4(15/2)	4(15/2)	10 k	10 k	4(15/2)	4(15/2)
R5	**R6**	**P7**	**P8**	**N1**	**N2**	**N4**	**P15**
20 k	20 k	2(15/2)	2(15/2)	4(5/4)	4(5/4)	(6/0.6)	(3/2)
N5	**P16**	**N6**	**P17**	**P11**	**P12**	**P13**	**P14**
(1.5/0.6)	(3/0.6)	3(1.5/0.6)	3(3/0.6)	16(9/3)	16(9/3)	16(9/3)	8(9/3)

Figure 6.50— Summing-comparator schematic.

Table 6.12— Summing-comparator specification compliance matrix.

Pins and Parameters	Target	WC Sim.	Expr.	Notes
Power supply	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V - 4.2 V	
ICMR Input Pair 1	0 V- (V_{DD}-1.5)	0 V- (V_{DD}-1.2)	0 V- (V_{DD}-1)	Worst case ICMR: V_{DD} = 2.7 V, Slow corner, 125 ˚C
ICMR Input Pair 2	0 - (V_{DD}-1.5)	0 - (V_{DD}-1.2)	0 V - (V_{DD}-1)	Worst case ICMR: V_{DD} = 2.7 V, slow corner, 125 ˚C
OUT, amplifier output Load drive capability	CMOS V_{Th}=V_{DD}/2	20 fF	10 pF	1X/3X Inverter logic
Quiescent Current	200 µA	278 µA	NA	Worst case: 1.2×I_{cc}
Comparator Delay (5 mV overdrive)	< 70 ns	42 ns	75 ns	High load at the output, 10 pF instead of 20 fF of sims
Input-Referred Offset (each input pair)	±20 mV	±11 mV	NA	Not critical

6.2.11. Driver and Dead-Time Controller (DTC)

Drivers are designed to amplify the driving capability of minimum sized logic gates for rapidly turning high gate capacitance, large, power MOSFETs on and off [105, 106]. The dead-time controller places a “dead-time” between turn-off and turn-on of power switches and ensures that power transistors are not enabled simultaneously at switching time to prevent *shoot-through* current that reduces the efficiency and damages the power MOSFETs (Figures 6.51 and Figure 6.52). Moreover, the driver should be strong enough to prevent turn-on of the low-side switch (M_L) through gate-drain capacitor, C_{GD}, coupling when the high-side switch is turning on (Figure 6.53).

A simple fixed-delay dead-time scheme (Figure 6.54) was used in the proposed chip where delay element pairs R_1 and C_1 and R_2 and C_2 create dead-time and ensure M_L turns on after M_H is turned off, and M_H turns on after M_L is turned off, respectively. The driver block input *In* is connected to the output of the RS latch in the current-mode controller and its outputs HGate and LGate are connected to gates of external high-side and low-side power MOSFETs, M_H and M_L. The driver is designed for typical turn-on and turn-off times of 15 ns with a 1 nF gate capacitance. Delay elements R_1 and C_1 and R_2 and C_2 are selected for a nominal 20 ns dead-time. During tuning and calibration, the driver unit is disabled by the digital core (i.e., NE=0), high-side gate HGate clamps to the

supply voltage, and the low-side gate LGate sticks to ground, and consequently, both power MOSFETs are turned off.

Experimental waveforms for the driver block driving an off-chip IRF7317 power MOSFET pair are shown in Figure 6.54. The driver circuit achieves dead-time of about 30 ns to 50 ns and rise and fall times of about 10 to 20 ns. The simulation and experimental results for this block are summarized in Table 6.13.

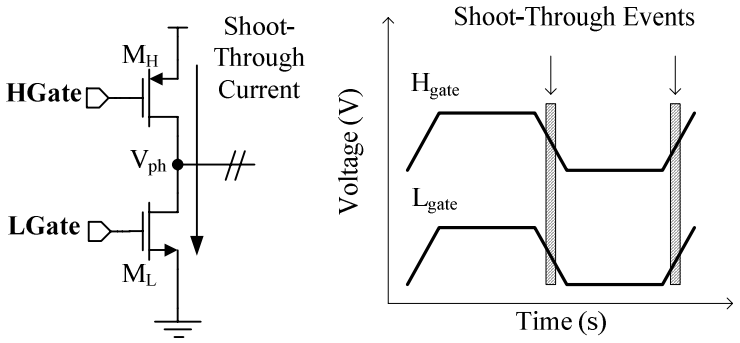


Figure 6.51— Shoot-through current as high-side and low-side power switches are turned on simultaneously during switching transients.

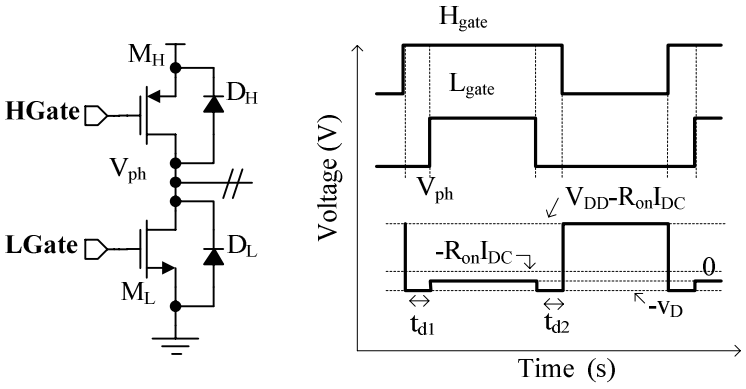


Figure 6.52— Including dead-time between turn-off and turn-on of power switches to prevent shoot-through current. Body diodes of switches may conduct currents at this dead-time.

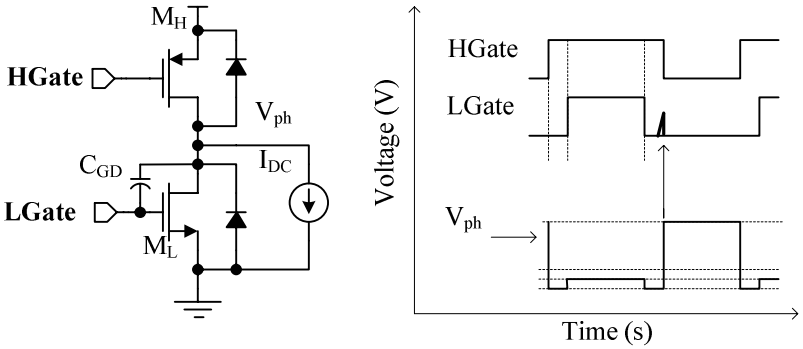


Figure 6.53— Turn-on of low-side power switch due to C_{GD} capacitor coupling as phase node rises may create large shoot-through currents if weak drivers are used.

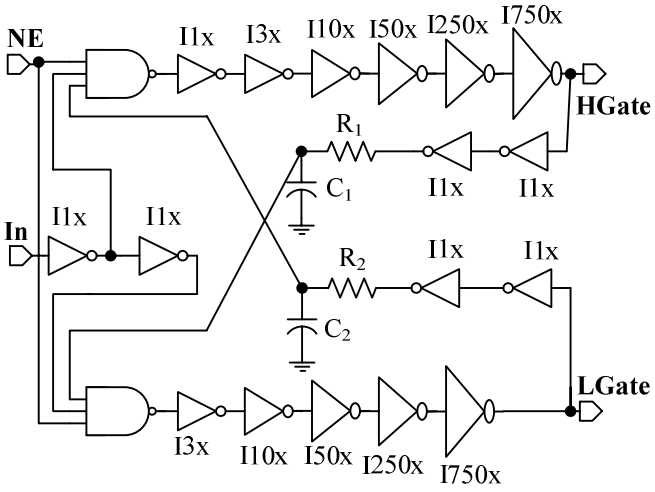
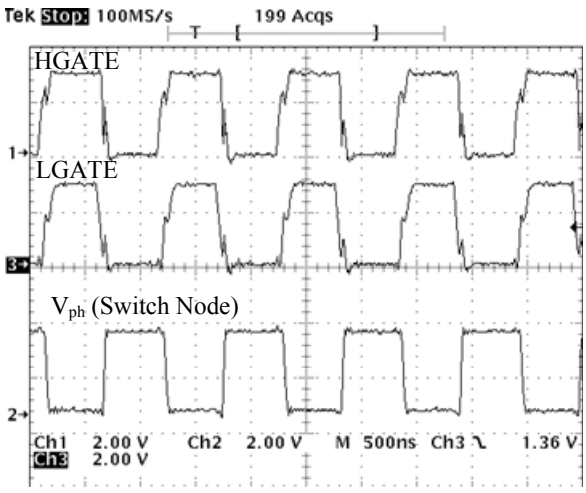


Figure 6.54— Driver and dead-time controller (DTC) circuit.

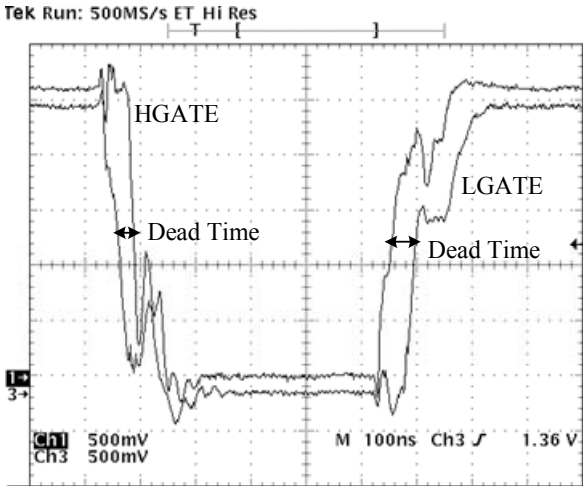
Table 6.13— Specification compliance matrix of driver and dead-time controller (DTC).

Pins and Parameters	Target	Nom. Sims	Expr.	Notes
Power Supply	2.7 V - 4.2 V	2.7 V - 4.2 V	2.7 V - 4.2 V	
HGate Rise Time 0.78 nF load	<20 ns	11 ns	20 ns	10% - 90% amplitude (1,2) V_{DD} = 2.7 V, IRF7317 switches
HGate Fall Time (0.78 nF load)	<20 ns	9.5 ns	10 ns	10% - 90% amplitude (1,2) V_{DD} = 2.7 V, IRF7317 switches
LGate Rise Time (0.9 nF load)	<20 ns	12.2 ns	20 ns	10% - 90% amplitude (1,2) V_{DD} = 2.7 V, IRF7317 switches
LGate Fall Time (0.9 nF load)	<20 ns	11.9 ns	10 ns	10% - 90% amplitude (1,2) V_{DD} = 2.7 V, IRF7317 switches
Dead-Time (DT) *From turn off of high-side to turn on of low-side*	10 ns < & < 50 ns	22 ns	30 ns	50% amplitude (1,3) V_{DD} = 2.7 V IRF7317 switches
Dead-Time (DT) *From turn off of low-side to turn on of high-side*	10 ns < & < 50 ns	30 ns	50 ns	50% amplitude (1,3) V_{DD} = 2.7 V IRF7317 switches

(1) IRF7318 C_{Hgat}=0.78 nF and C_{Lgate}=0.9 nF. For simulations C_{Hgate}=0.59 nF and C_{Lgate} =0.73 nF.
(2) Rise and fall times are 10%-90% numbers for simulations and 0-50% rise time for experimental results.
(3) Dead-time from 50% of the first signal to the 50% of the second signal. The experimental numbers for gate capacitors are derived from switch datasheets. The simulation numbers are taken from DC operating point of C_{gs} in the switch models provided by the IRF, switch manufacturer.



(a)



(b)

Figure 6.55— Measured high-side gate (HGATE), low-side gate (LGATE), and phase node waveforms. Zoomed (a) out and (b) in.

6.2.12. Digital Core

The digital core is responsible not only for directing the tuning and calibration but also for reliable start-up of the DC-DC converter. The start-up sequence is planned as follows and is illustrated in Figure 6.55. Just after the power-on-reset, tuning starts by forcing a 50 mA peak-to-peak current, and an approximately 30 mA DC triangular current into the inductor. However, the g_m-C filter operates reliably only if its main negative input, connected to the converter output node, exceeds 0.6 V. As discussed before, the test current generator circuit ensures that output voltage V_o reaches about 0.9 V during turning and calibration. Because of a 47 μF capacitor at the output, there is a delay before the output capacitor ramps up to 0.9 V and the output reaches steady state. The digital core uses an internal comparator to detect the point when V_o exceeds 0.8 V, and then enables the tuning measurements. When transconductance g_m of the g_m-C filter exceeds its targeted value, tuning stops and the tuning circuit acknowledges the event to the digital core. Then, power-on-reset disables tuning block and enables calibration. When resistor R of the g_m-C filter exceeds its targeted value, calibration stops and the event is acknowledged to the digital core. At this point, the g_m-C filter is adjusted for accurate current measurement and the digital core permits converter normal converter operation. Note however that, as discussed, the switching regulator starts up in a soft-start mode for a reliable transition to normal operation.

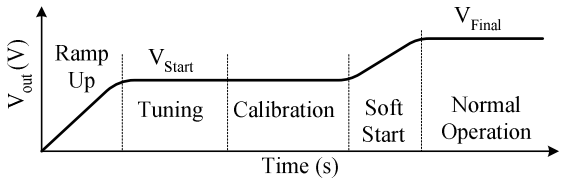


Figure 6.56— Buck converter output voltage during start-up sequence.

Table 6.14 summarizes the transitions that occur during start-up from tuning to calibration and then to normal operation. Figure 6.57 shows the complete digital core circuit implementation. AOI2 is an AND-OR combinational logic. The trigger blocks are one-shot generators. To facilitate testing, an engineering test mode was devised that can put the chip through tuning only, calibration only, or normal operation only, controlled by

test-mode pins T1 and T2. The RST pin can trigger a power-on-reset event to test the start-up without powering the chip down and up.

Table 6.14— Description of the transient events at start-up.

Transitions	Events
Power-on-Reset → Tune	- Bandgap is powered on - Wave generator is reset - Wave generator is put in triangular-signal-generation mode - Test current generator is enabled - Tuning and calibration counters are reset - G_m-C filter offset cancellation clock resets adding enough time for the offset-cancellation circuit to stabilize before any processing
Tune → Calibration	- Wave generator is reset - Wave generator is put in ramp-generation mode - Calibration counter is reset - G_m-C filter offset cancellation clock resets adding enough time for the offset cancellation circuit to stabilize before any processing
Calibration → Normal Operation	- Current-mode controller is enabled - Test-current generator is disabled

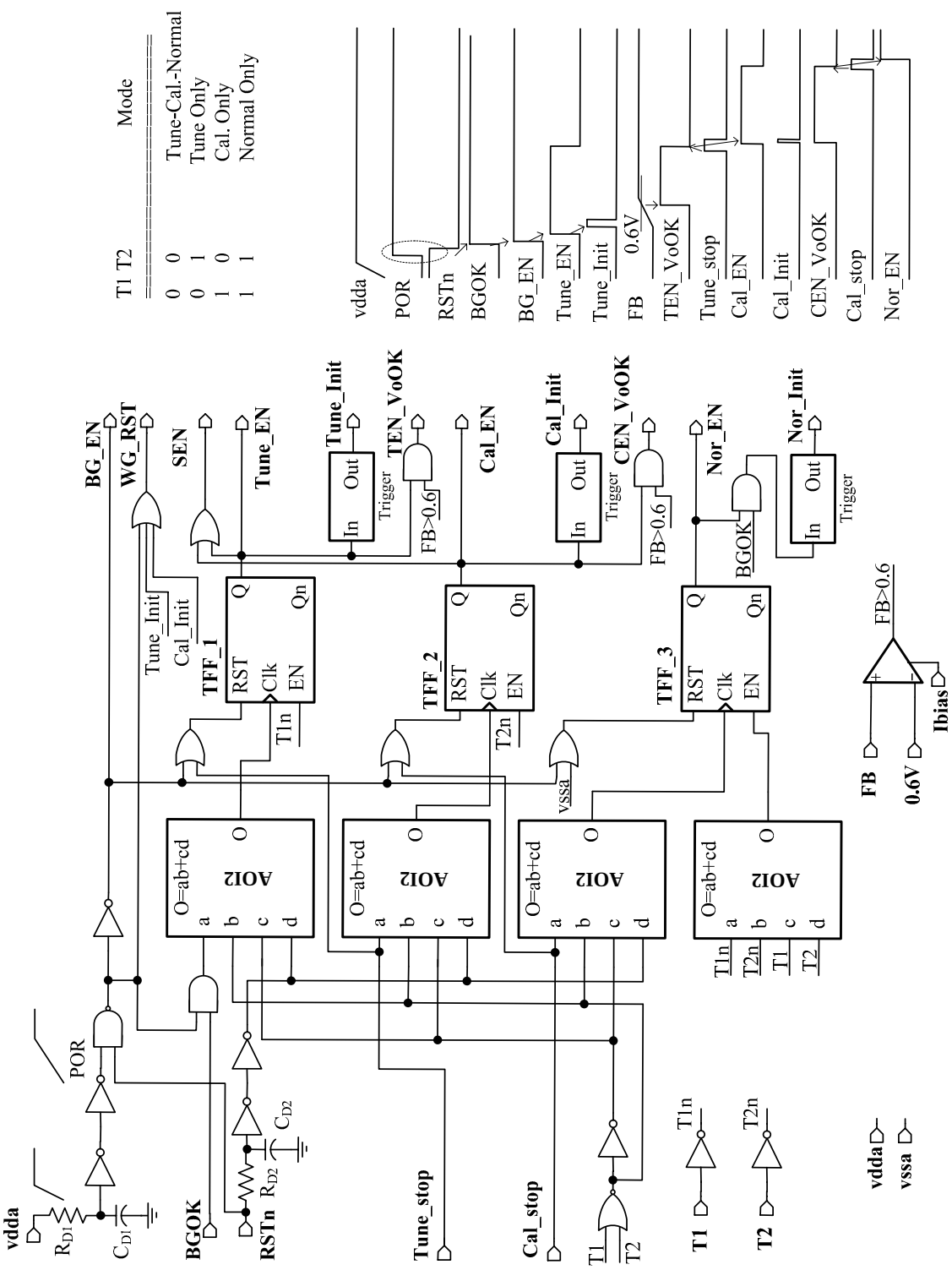


Figure 6.57— Digital-core schematic.

6.2.13. Voltage Reference Network and Bias Generator

This block, the circuit schematic of whichis illustrated in Figure 6.58, provides voltage references and bias currents for all the other circuits. The bandgap voltage is not generated on-chip, and an external voltage reference is used. This voltage reference is connected to the *Vrefin* input pin, and internal voltages references are then constructed through the amplifier A_{Ref}, which is a two-stage amplifier, and resistor divider R1 through R11. Resistors Ra and Rb and transistors Na and Nb provide a crude bias circuit for the amplifier. Three of the outputs, *Vcal*, *Vlt* and *Vht*, which ultimately are connected to the current generator block inputs, are referenced to the positive supply rail. Bias currents are generated by putting a 1.4 V voltage supply across resistor R_c, which is an external resistor to give more flexibility during the test (i.e., bias currents can be varied). The stage is compensated with the output capacitor C_{out}. However, it was found that this compensation scheme leads to instability for bias currents since any noise or coupling on *Vrefin* is amplified at the gate of transistors N1 and N2. This would effectively limit the operation range of the circuit from 2.7 V to 3.5 V. A better compensation for this circuit uses a miller compensation for the two-stage amplifier A_{Ref}. The *BGEN* input is an enable signal that comes from digital core after power-on-reset and *BGOK* is an output that trips once the *Vref(1V)* output has reached its steady-state value after a reset (i.e., there is a delay until external capacitor C_{out} is charged). The block specification compliance matrix is provided in Table 6.15. Only the *Vref(1V)* output is measured since other outputs are internal.

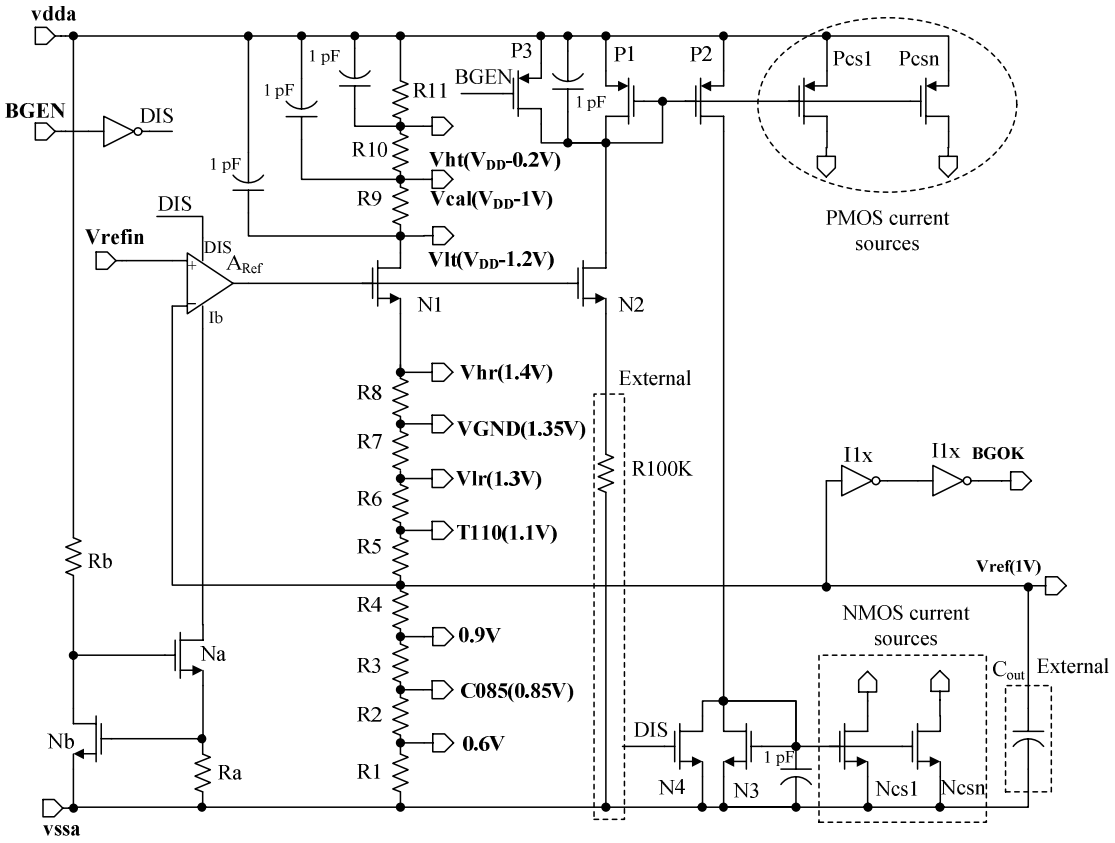


Figure 6.58— Schematic of voltage reference and bias generator circuit.

Table 6.15— Specification compliance matrix of voltage reference and bias network.

Pins and Parameters	Target	Nom. Sim.	Expr.	Notes
Power Supply (V_{DD})	2.7 V - 4.2 V	2.7 V - 4.2 V	2.6 V- 3.5 V	Stability problem forces the operation to low voltage levels
V_{cal}, Cal. voltage for test current generator	1 V to supply	V_{DD} - 1 V		±1% accuracy is required
V_{ref} , reference voltage for error amplifier	1 V to gnd	1 V	1 V ±4 mV	Based on 5 samples ±1% accuracy is required
V_{Hr}, ramp high-voltage limit to wave generator	1.3 V to gnd	1.3 V		±10% accuracy is required
V_{Lr}, ramp low-voltage limit to wave generator	1.4 V to gnd	1.4 V		±10% accuracy is required
V_{Ht}, tri. high-voltage limit to wave generator	0.2 V to supply	V_{DD} - 0.2 V		±1% accuracy is required
V_{Lt}, tri. low-voltage limit to wave generator	1.2 V to supply	V_{DD} - 1.2 V		±1% accuracy is required
V_{refH}, reference high voltage	1.1 V to ground	1.1 V		±10% accuracy is required
V_{refL}, reference low voltage	0.9 V to gnd	0.9 V		±10% accuracy is required
0.6V, start-up	0.6 V ±1%	0.6 V		±10% accuracy is required
Quiescent Current	-	83 µA	NA	

6.2.14. Temperature-Compensation Circuits

As it was discussed in Chapter 4, the inductor ESR change with temperature causes significant errors in DC values in the current-sensing filter. From Figure 6.1, the DC output voltage of the g_m-C filter is

$$V_{Sense} = ((g_mR)R_{ESR})I_L. \quad (6.24)$$

From g_m-C filter implementation in Section 6.2.1, the value of the transconductance g_m is K/R_1, where K is the current mirror ratio, and almost temperature independent. Both resistors R and R_1 are implemented with the same poly-silicon resistors, which have a relatively low temperature coefficient (i.e., -300 ppm/°C), and therefore, filter gain (g_mR) remains almost constant with temperature. However, resistor R_{ESR} is an strong function of temperature whose relation is given by

$$R_{ESR} = R_{ESR0}(1+\alpha(T-T_0)), \quad (6.25)$$

where α is the ESR temperature coefficient (TC), which is 3900 ppm/°C for copper; T is the temperature; and R_{ESR0} is the value of ESR at temperature set point T_0. To compensate for the effect of temperature, $(g_mR)R_{ESR}$ should be constant, and therefore, g_m and R should be redesigned such that low-frequency gain (g_mR) has a negative temperature coefficient of -3900 ppm/°C. This solution, however, is not attractive because of the complexity involved.

A simpler method to compensate for temperature variations is to change the way the current-sensing output is used in the system. For example, if the peak value of the current-sensing filter output is used for the over-current protection, use of a PTAT voltage source (V_{level} in Figure 6.59(a)) instead of a constant voltage reference at the negative input of the comparator compensates for ESR temperature effects. To make this method effective, the calibration voltage V_{cal}, which sets the value of g_mR in calibration loop, should be PTAT as well (Figure 6.59(b)). The temperature compensation circuits were not implemented in IC prototype.

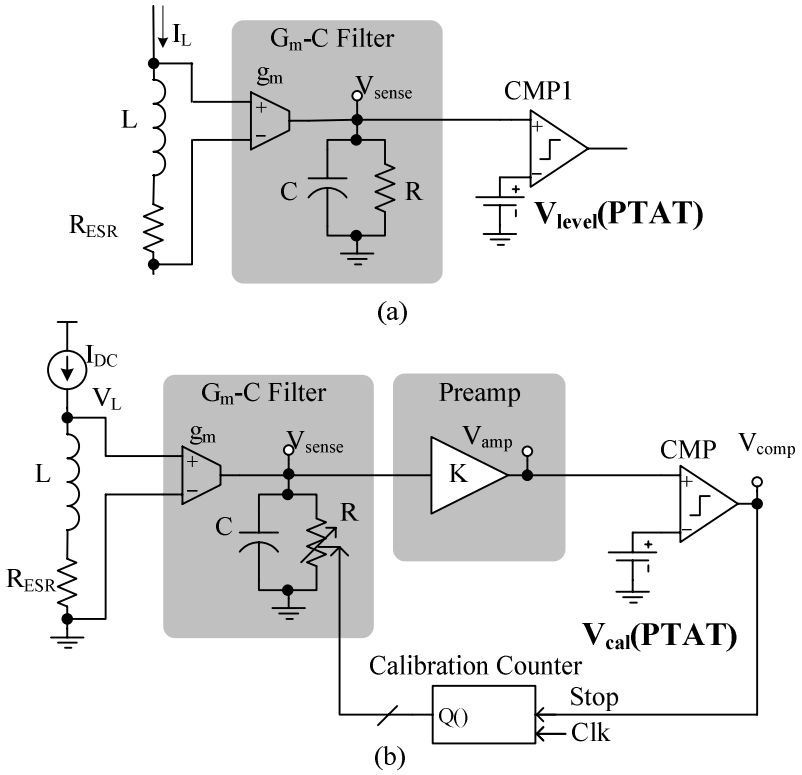


Figure 6.59— To compensate for the ESR temperature coefficient, PTAT voltage sources can be used in both (a) application and (b) calibration circuits.

6.3. Final Chip

Thus far, the design of individual building-block circuits in the proposed IC was discussed. This section discusses how these blocks were connected together to form the system. After discussing the system design strategy briefly, top-level design of the final chip is presented. Then the top-level simulation plan is provided and the floorplan and layout of the final chip are offered.

6.3.1. Design Cycles

The design of the whole system was performed in two design cycles, where three test chips were submitted in each tape-out. First-cycle tape-out was performed to investigate the design and performance of critical blocks such as the g_m-C filter and the calibration loop. This run proved quite useful in catching several circuit bugs such as an incorrect connection in the g_m-C filter layout, which was not caught by Diva LVS.

The second design cycle included the whole system (final chip), but current-sensor (g_m-C filter, tuning loop, and calibration circuit) and current-mode controller subsystems were also implemented on separate chips where more pins could be dedicated for test purposes. The design cycles, chips taped out, and their respective areas are summarized in Table 6.16. The rest of discussion focuses on top-level design of the final chip.

Table 6.16— Summary of design cycles.

Design Cycles	Chip No.	Blocks Implemented	Chip Area
1	1.1	G_m-C Filter	1.5 mm x 1.5 mm
	1.2	Calibration	1.5 mm x 1.5 mm
	1.3	AZ_Comp, Preamp, Error Amplifier	1.5 mm x 1.5 mm
2	2.1	Final Chip (Current Sensor and Current-Mode Controller)	3 mm x 1.5 mm
	2.2	Current-Mode Controller	1.5 mm x 1.5 mm
	2.3	Current Sensor	1.5 mm x 1.5 mm

6.3.2. Final Chip Top Level

The final chip symbol and schematic are shown in Figures 6.60 and Figure 6.61, respectively. The top-level circuit mainly consists of g_m-C/tune/cal (i.e., current sensor), current-mode controller (Section 6.2.8), I_{test} current generator (Section 6.2.6), wave generator (Section 6.2.7), reference and biasing (Section 6.2.13), and digital core (Section 6.2.12). The g_m-C/tune/cal block top-level, which includes g_m-C filter (6.2.1), tuning loop (6.2.2), and calibration circuit (6.2.3), is shown in Figure 6.62. The chip uses two separated pins, vdda and vddd, for analog and digital power supplies and three separated analog, digital, and high-current analog grounds (i.e., vssa, vssd, and vssaHC). The high-current ground is used for the current generator since it conducts up to 50 mA of current at start-up. The final chip pin assignments and descriptions are given in Table 6.17.

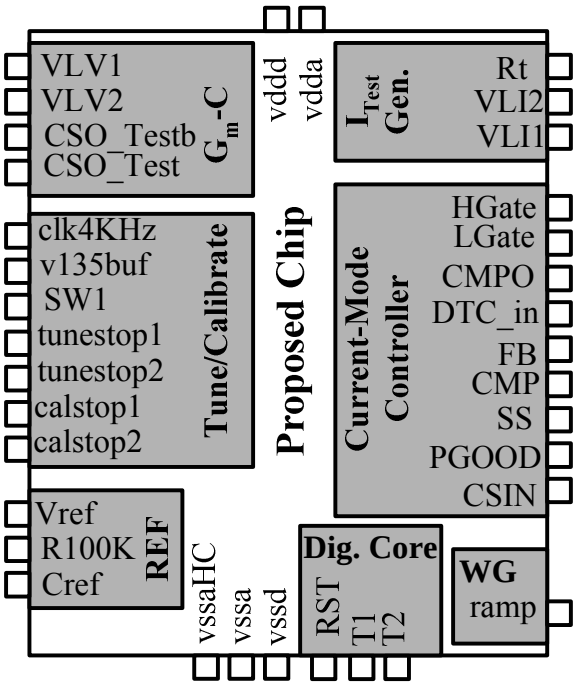


Figure 6.60—Final chip symbol.

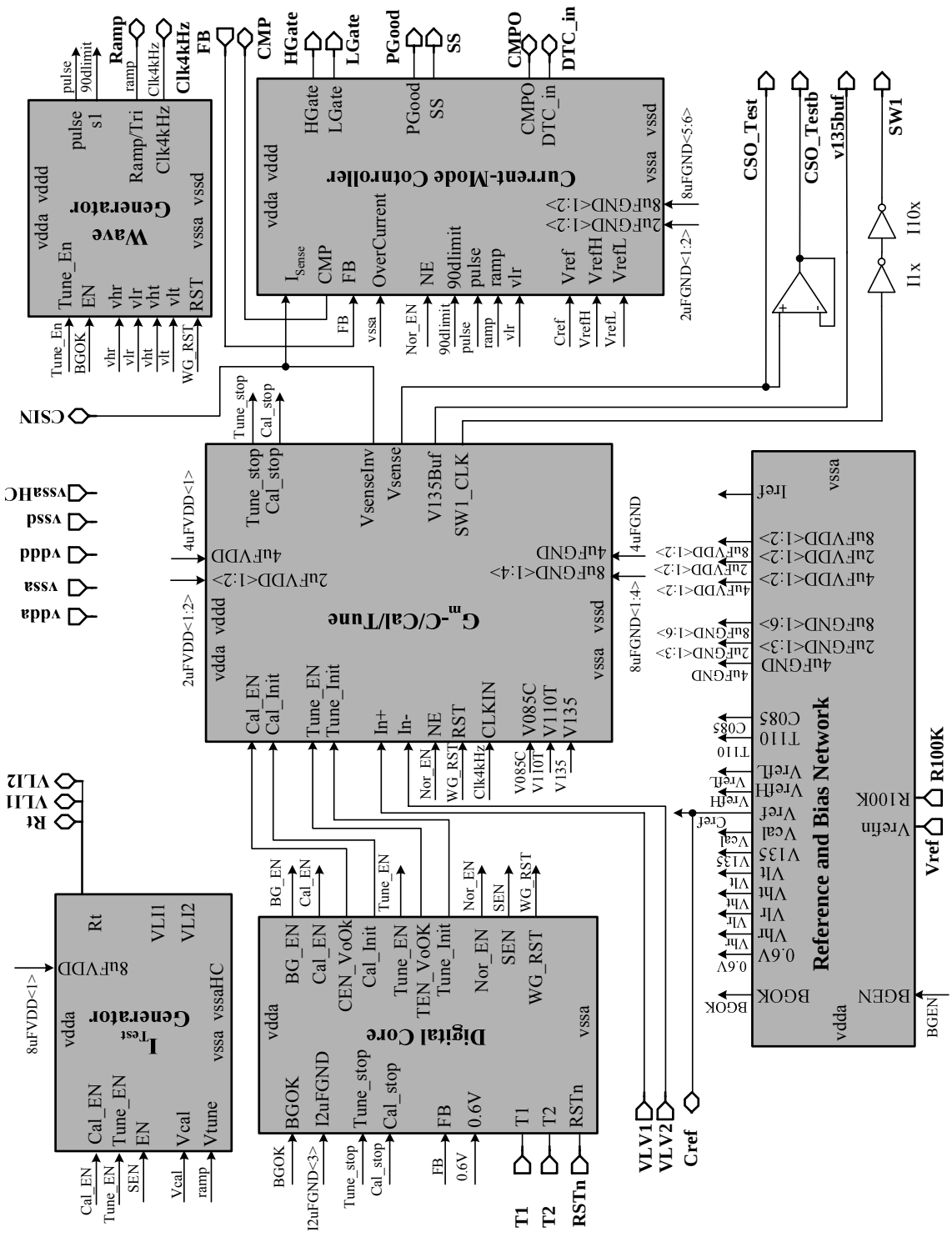


Figure 6.61— Final chip top-level schematic.

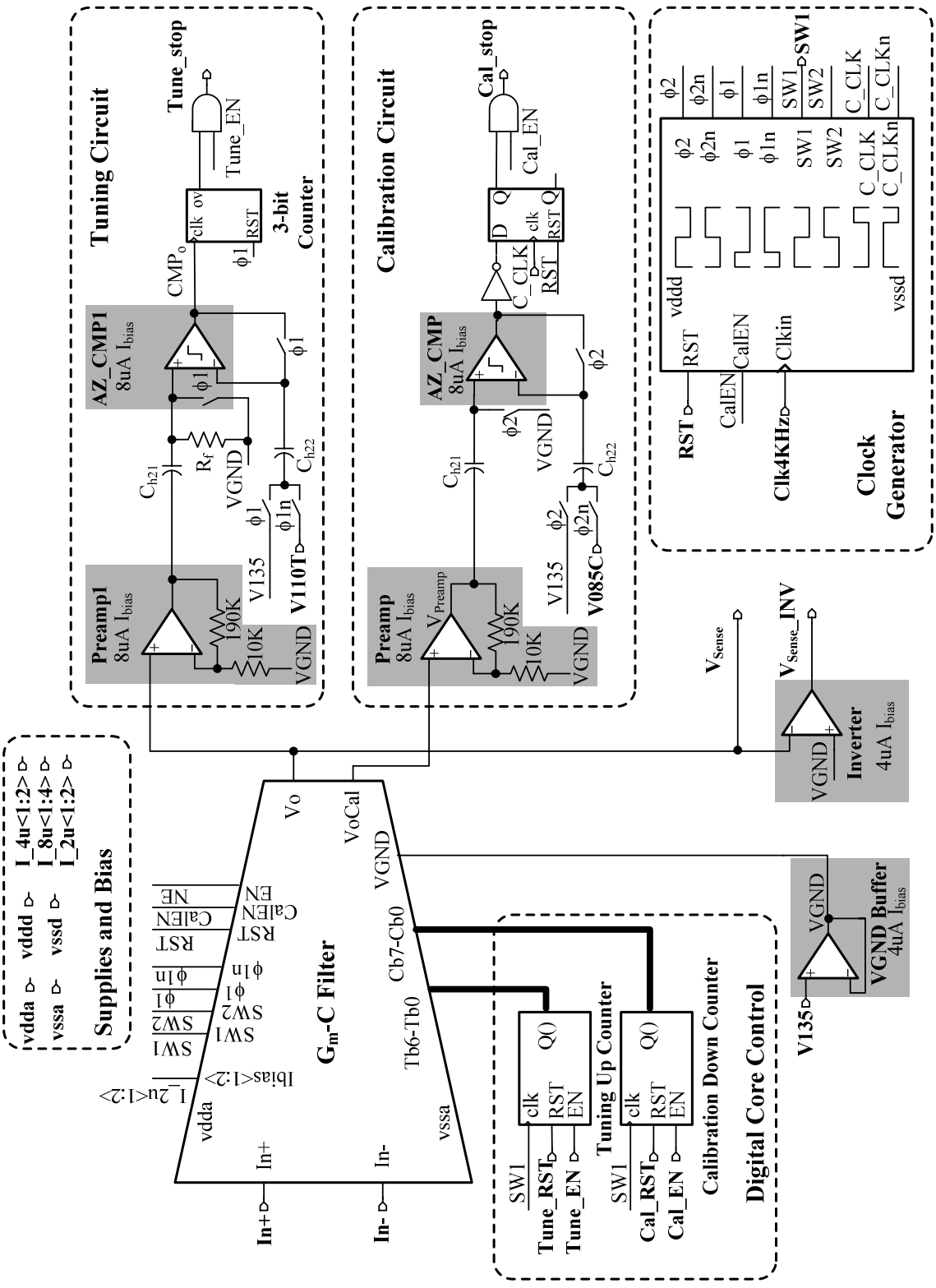


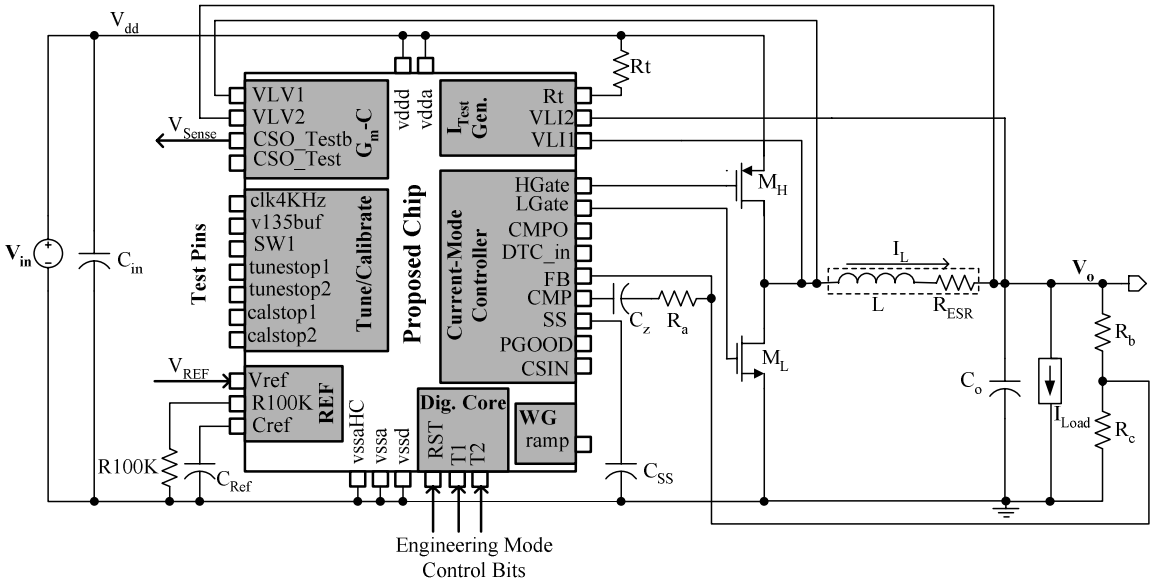
Figure 6.62— G_m-C/Tune/Cal (current sensor) block top-level schematic.

Table 6.17— Final-chip pin description.

Pin Name	Pin Group	Description
vdda	Supply/GND	Analog power supply
vddd	Supply/GND	Digital power supply
vssa	Supply/GND	Analog GND
vssd	Supply/GND	Digital GND
vssaHC	Supply/GND	High current (50mA) analog ground
VLV1	G_m-C	Inductor switching node sense point (G_m-C filter positive input)
VLV2	G_m-C	Inductor output voltage sense point (G_m-C filter negative input)
CSO_Test	G_m-C	V_{Sense} (G_m-C filter output)
CSO_Testb	G_m-C	V_{Sense} buffered (G_m-C filter output buffered with an internal buffer)
Clk4KHz	Cal/Tune	Test point, 4 kHz master clock for auto zeroing
V135buf	Cal/Tune	Test point, 1.35 V buffered
SW1	Cal/Tune	Test point, SW1 clock of auto zeroing
Tunestop1	Cal/Tune	Test point, tune comparator output
Tunestop2	Cal/Tune	Test point, tune comparator output (connected internally to Tunestop1)
Calstop1	Cal/Tune	Test point, calibration comparator output
Calstop2	Cal/Tune	Test point, calibration comparator output (connected to Calstop1)
RST	Digital Core	Operation reset
T1	Digital Core	Engineering test mode bit 1
T2	Digital Core	Engineering test mode bit 2
Ramp	Wave Generator	Test point , ramp/triangular waveform generator output
HGate	Regulator	Test point, high-side MOSFET gate drive
LGate	Regulator	Test point, low-side MOSFET gate drive
CMPO	Regulator	Test point, summing comparator output
DTC_in	Regulator	Test point, driver/dead-time controller input
FB	Regulator	Feedback node (error amplifier negative input)
CMP	Regulator	Compensation node (error amplifier output)
SS	Regulator	Soft-start capacitor connection
PGOOD	Regulator	Power good, enables if V_o is within ±10% of its desired range
CSIN	Regulator	Summing comparator current-sensing input Connected internally to inverted output of g_m-C filter
Rt	I_{Test} Generator	Test current generator resistor connection. 20Ω for 50mA
VLI1	I_{Test} Generator	Test current generator current source
VLI2	I_{Test} Generator	Test current generator current sink
Vref	Reference and Bias	Input reference voltage
R100K	Reference and Bias	Bias current reference resistor
Cref	Reference and Bias	Voltage reference network compensation capacitor input

6.3.3. Top-Level Simulation Plan

Top-level simulation of complex, mixed-signal circuits is a challenge by itself. Simulation of switching regulators usually requires about 1000 switching cycles to validate the start-up of the converter. Therefore, these simulations are time- consuming and special tricks should be used as discussed in Appendix A. The simulation time is even worse for tuning and calibration loops since they operate at much lower frequency than the main system clock frequency (i.e., 1 kHz versus 1 MHz) and several operation cycles (up to 512) are needed for calibration and tuning loops to converge. Consequently, to simulate the circuit behavior completely, transient simulation up to 500 ms of operation may be necessary, which can take up to few weeks on available computational resources (i.e., computationally impossible) if transistor-level models are used. To circumvent this problem, the connection of tuning and calibration counters to g_m-C filter was modified to just include 2 bits instead of actual 7 and 8 bits for programmable transconductance and resistor, and therefore the tuning and calibration circuits can conclude in four operating cycles (i.e., 8 ms simulation time). To reduce the simulation time further, behavioral and functional modes were used for the digital core and wave generator. The digital core engineering mode bits T1 and T2 were also set up to put the chip in calibration only, tuning only, or current-mode controller only modes and speed up the simulations. The final chip simulation circuit setup is shown in Figure 6.59.



R_a	R_b	R_c	C_z	C_{ss}	Rt
15 kΩ	1 kΩ	2 kΩ	20 nF	2 nF	20 Ω
L	**R_{ESR}**	**C_o**	**V_{REF}**	**C_{Ref}**	**R100k**
3.9 µH	50 mΩ	47 µF	1 V	1 nF	100 kΩ

Figure 6.63— Final-chip simulation setup.

6.3.4. Layout

Experienced designers always say that a high-performance circuit is as good as its physical design. Extreme care and time were dedicated to perform the layout of the final chip. Analog layout techniques were applied where necessary for improving matching of matched devices, reducing the capacitive coupling between noisy and sensitive nodes, and eliminating IC failure mechanisms such as electro-migration, latch-up, minority injection, and antenna effect [105, 106]. The final complete floorplanning along with pin assignments is shown in Figure 6.61 and the chip photograph in AMI's 0.5-µm CMOS process is offered in Figure 6.62. The areas of individual blocks are listed in Table 6.18. More discussion on layout strategies for switching regulators is provided in Appendix B.

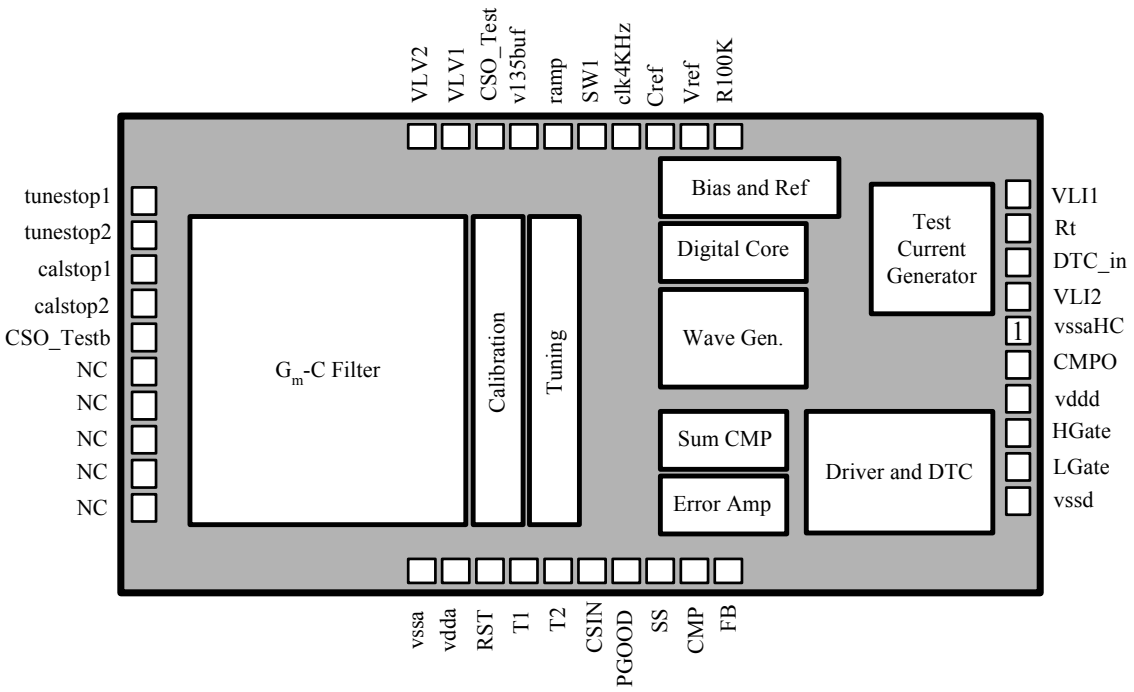


Figure 6.64— Final-chip complete floor plan and pin locations.

Table 6.18— Layout area of the key blocks of the proposed IC in AMI's 0.5-µm CMOS process.

Unit	Area
Whole Chip	1.500 mm x 3.000 mm
G_m-C Filter	0.878 mm x 0.890 mm
Tuning	0.890 mm x0.157 mm
Calibration	0.890 mm x 0.157 mm
AZComp (including hold capacitors)	0.411 mm x 0.157 mm
Preamp (including resistors)	0.235 mm x 0.157 mm
Wave Generator	0.524 mm x 0.300 mm
Voltage Network and Bias	0.538 mm x 0.132 mm
Error amplifier	0.260 mm x 0.160mm
Summing Comparator	0.270 mm x 0.140 mm
Drivers and DTC	0.508 mm x 0.308 mm
Test Current Generator	0.290 mm x 0.480 mm
Control logic	0.415 mm x 0.190 mm

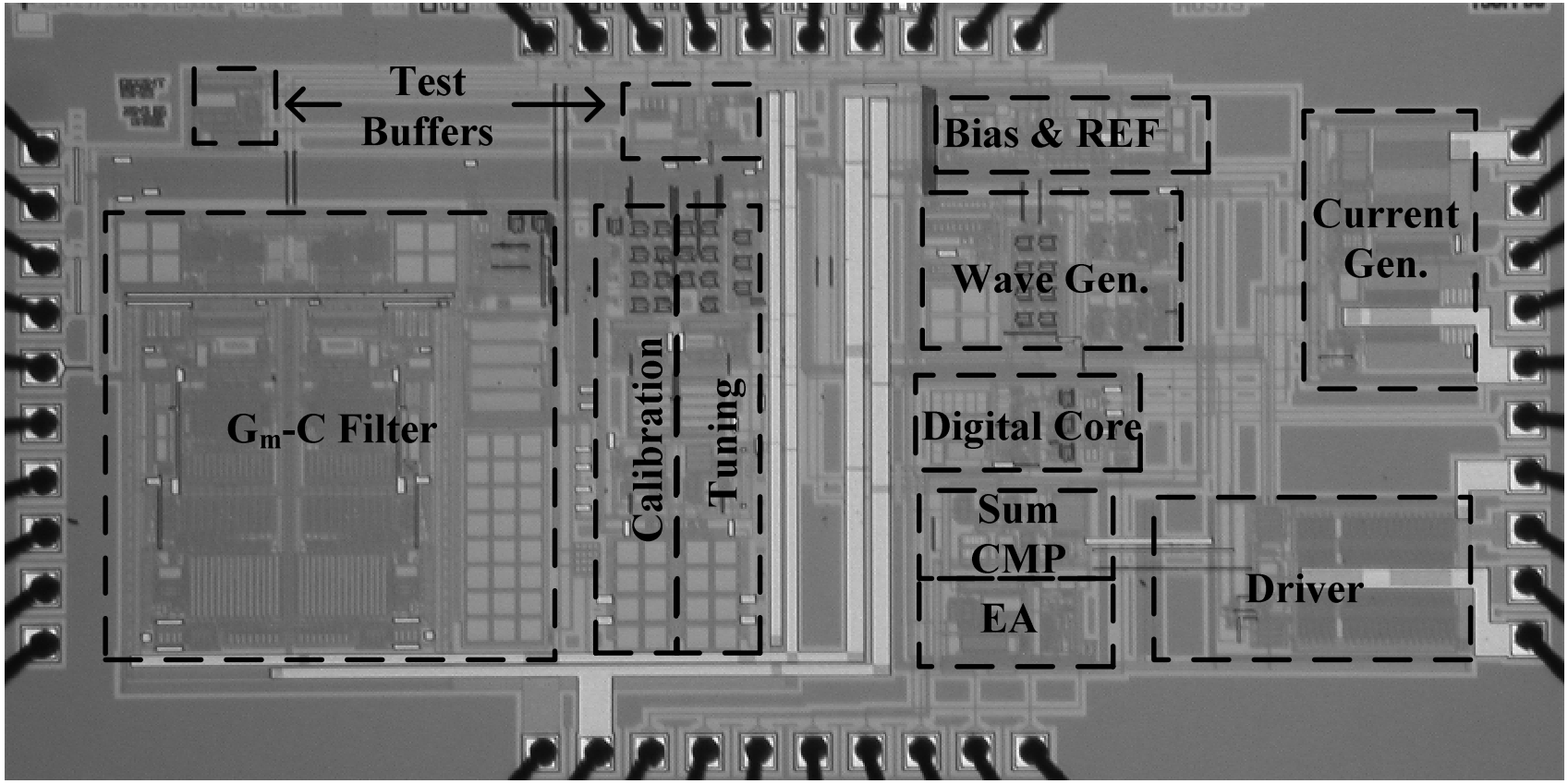


Figure 6.65— Final chip photograph implemented in AMI's 0.5-μm CMOS process.

SUMMARY

This chapter discussed a prototype circuit implementation for the proposed current-sensing technique and its current-mode controller test bed in the CMOS AMI's 0.5-μm process. The chapter started with system-level hierarchy, presented individual circuit block implementation, and discussed simulation and test results. The chapter concluded with a discussion of design, simulation, and layout of the final chip. The next chapter presents the final chip test setup and discusses the system-level experimental results.

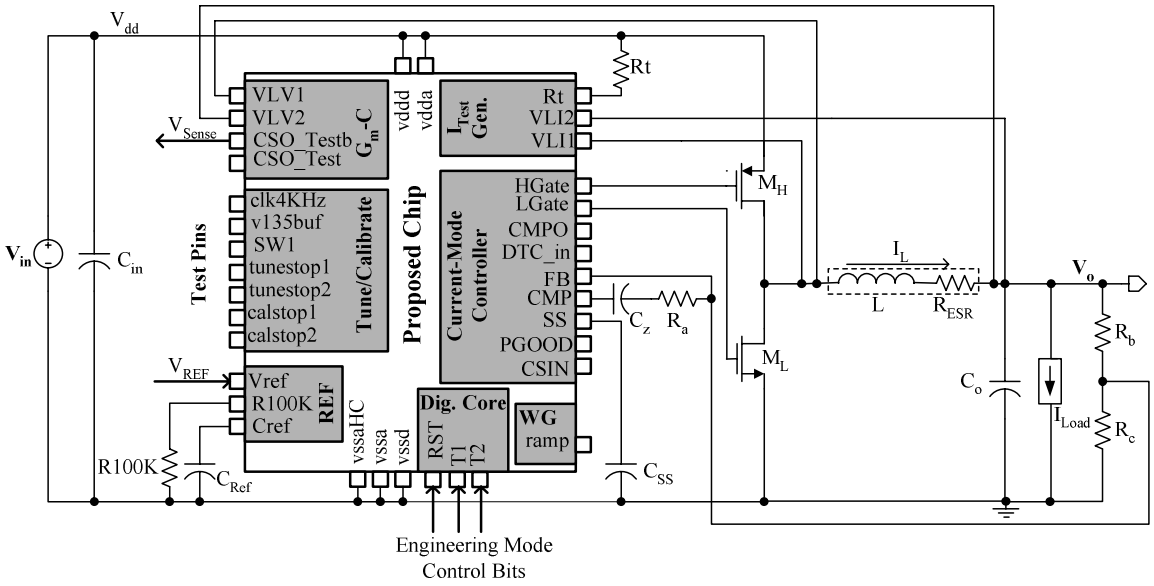
CHAPTER 7

SYSTEM EXPERIMENTAL EVALUATION

Debugging and characterizing the fabricated integrated circuits is an important and tedious stage of the design cycle. In this chapter, design of the evaluation board (EVB) for the final chip is discussed. Then, the experimental evaluation results of the fabricated final chip, which includes proposed current-sensing technique and current-mode buck DC-DC converter, are presented. The focus of this chapter is on the system evaluation rather than on individual blocks, which were presented in the previous chapter. The chapter concludes by discussing the issues of the final chip and suggesting fixes to address them.

7.1. Test Bed

To test the fabricated final chip, an evaluation board (EVB) was designed and fabricated. The board schematic is shown in Figure 7.1 and the photograph of the assembled board is illustrated in Figure 7.2. In addition to the proposed chip, a 1.25 V reference IC (REF7317) and a quad amplifier IC (MAX4234) were placed in the board to provide an external reference and off-chip buffers, respectively. The external power stage consisted of an IRF7317 power switch pair IC, an inductor, and a capacitor. One of the amplifiers in MAX4232 was used to implement a differential amplifier with gain of 10. When the inputs of this differential amplifier were connected to the ports of a 50 mΩ sense resistor placed in series with the inductor, a 0.5 V/A external current-sensing circuit was created that could be used to characterize the proposed current-sensing technique. Several test points and jumpers were set up on the EVB to facilitate characterization and debugging. For simple part replacements, a socket was put on the EVB to hold the final chip package, which was assembled in a 40-pin dual-in-line (DIP40) package. Since the power stage is to be implemented off-chip, the circuit was less sensitive to the DIP40 package and socket parasitic.



R_a	R_b	R_c	C_z	C_{ss}	Rt
15 kΩ	1 kΩ	2 kΩ	20 nF	2 nF	20 Ω
L	**R_{ESR}**	**C_o**	**V_{REF}**	**C_{Ref}**	**R100k**
3.9 µH	50 mΩ	47 µF	1 V	1 nF	100 kΩ

Figure 7.1—Evaluation board schematic.

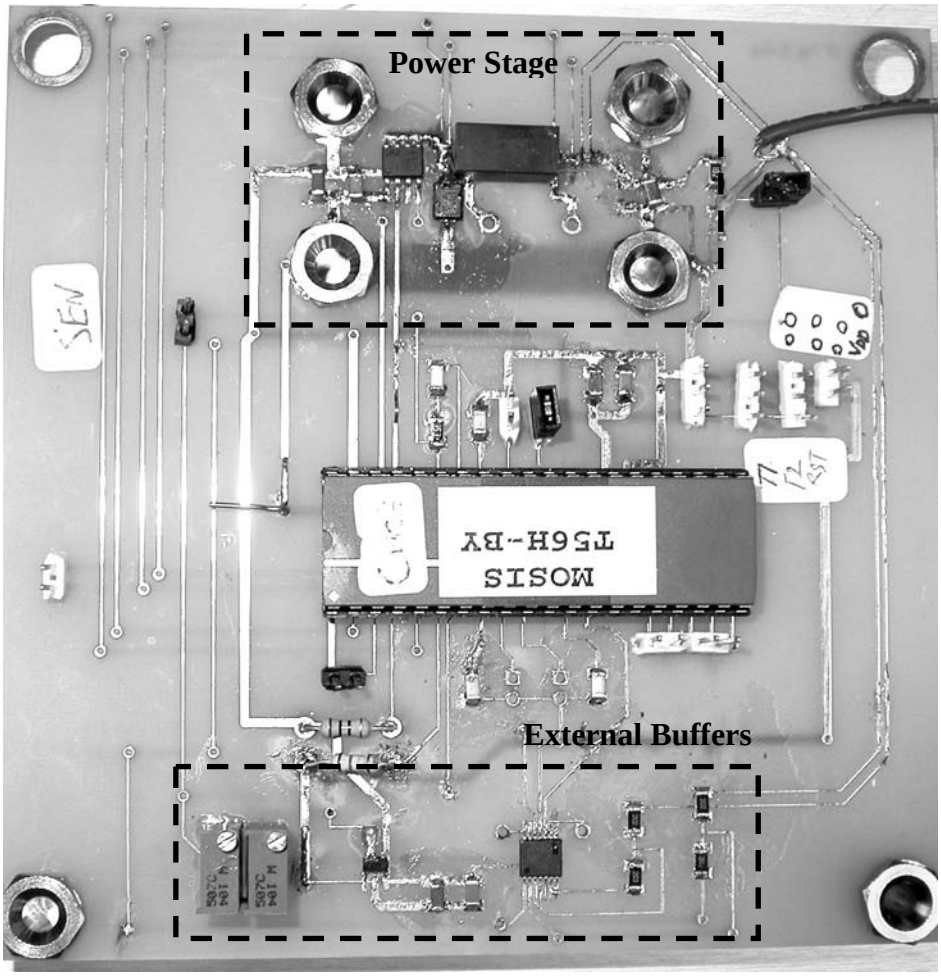


Figure 7.2—Evaluation board (EVB) photograph.

7.2. Test Instruments

An oscilloscope was used to characterize and debug the final chip, as most power-management chips use this instrument for these tasks [107-109]. Power supplies and active loads were used to force input voltage and load current, and accurate multimeters were used to measure DC voltages and currents. To resolve some issues, a probe station with a laser cutter was used to test internal signals and to reconfigure circuit topologies.

7.3. System-Level Experimental Results

The proposed IC was fabricated in AMI's 0.5-µm CMOS process through MOSIS. The off-chip elements include the power stage (i.e., L = 3.9 µH, C_o = 47 µF and power switches (IRF7317) with typical 65 mΩ and 27 mΩ resistances for PMOS and NMOS switches, a current-mode controller compensation network (i.e., R_a = 15 kΩ,

R_b = 1 kΩ, R_c = 2 kΩ, and C_z = 20 nF), and a soft-start capacitor (i.e., C_{SS} = 2 nF) (Figures 7.1 and 6.63).

To speed up the calibration, the digital core was designed to disconnect from g_m-C filter capacitor C; however, doing so had the adverse effect of increasing noise at the filter output and interfered with the calibration accuracy. To reduce the noise in the calibration loop due to removal of the filter capacitor, an external RC low-pass filter was placed at the output of the calibration comparator, which was accessible through pins (more discussion in Section 6.1.3). Therefore, the setup of Figure 7.1 was changed accordingly for calibration loop performance characterization. All other system-level measurements were performed on basic setup of Figure 7.1.

To evaluate the AC response of the current-sensing technique, a 50 mΩ sense resistor and a differential amplifier with gain of 10 was used to achieve a reference 0.5 V/A current measurement. For DC current evaluation, an ammeter was used to read the DC load current, which is equal to inductor current. For a typical operation test, the system was tuned and calibrated by using the tuning and calibration algorithms discussed earlier, and normal operation was then tested using a 3.9 μH, 48 mΩ ESR inductor. The experimental continuous-output ripple current response of the circuit matches the reference sense-resistor ripple current with an AC error of less than -9%, as shown in Figure 7.3 and depends on tuning-circuit performance. Measurement of DC value of current, however, depends on the calibration process, and the results shown in Figure 7.4 were recorded while varying the inductor current by changing the load current from 0 A to 0.8 A in 0.1 A steps. The thin line is the targeted 0.5 V/A gain and the bold trace is the experimental result for calibrated filter R for 0.5 V/A gain. The experimental curve starts below the ideal curve due to the nonlinearity of g_m-cell and the resulting systematic offset (Chapter 6.1 and Chapter 6.4) [73] and maintains an error of less than 8% through the range of currents.

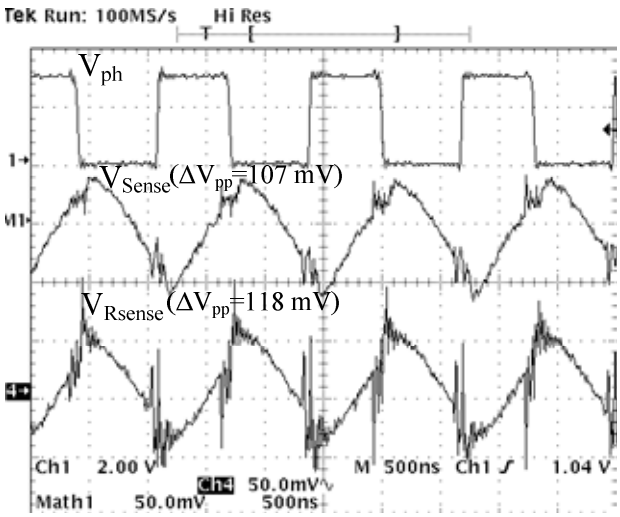


Figure 7.3—Measured AC inductor current using the proposed (V_{sense}) and sense resistor (V_{Rsense}) techniques. Switching node (V_{Ph}) is also shown ($L = 3.9\ \mu H$, $R_{ESR} = 48\ m\Omega$, $V_{in} = 3\ V$, $V_o = 1.5\ V$).

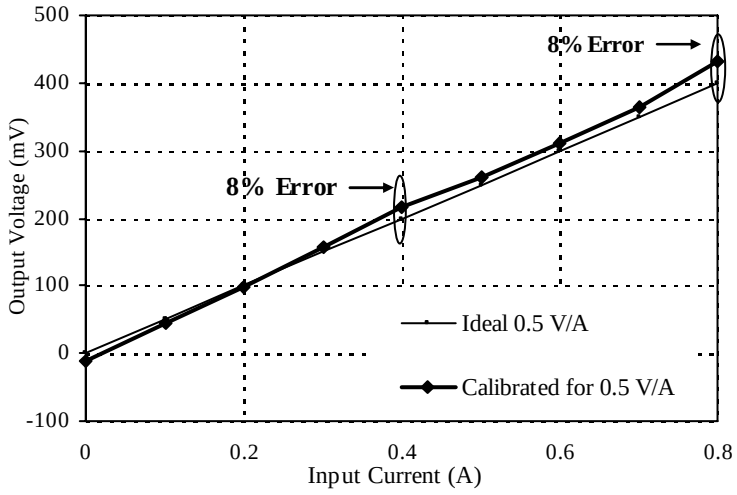


Figure 7.4—Calibrated DC current-sensing gain versus ideal characteristic ($L = 3.9\ \mu H$, $R_{ESR} = 48\ m\Omega$).

The worst-case effects of ping-pong transitions on g_m-C filter output are small, as shown in Figure 7.5. Although a 40 mV transient glitch shortens the duty cycle of its occurrence switching period at the transition of the ping-pong clock (SW1), its effect is compensated in the next switching period. The experimental results confirm a bandwidth adjustment from 1.1 kHz to 6.4 kHz and DC gain variation from 1.27 V/V to 29.16 V/V. Typical filter frequency response is given in Figure 7.5 for one nominal and two extreme

cases. The bandwidth and gain resolution are guaranteed by design and verified by simulations at 3.2% (5 bits) for worst-case conditions, which is when resistor R or transconductance g_m is at its minimum value.

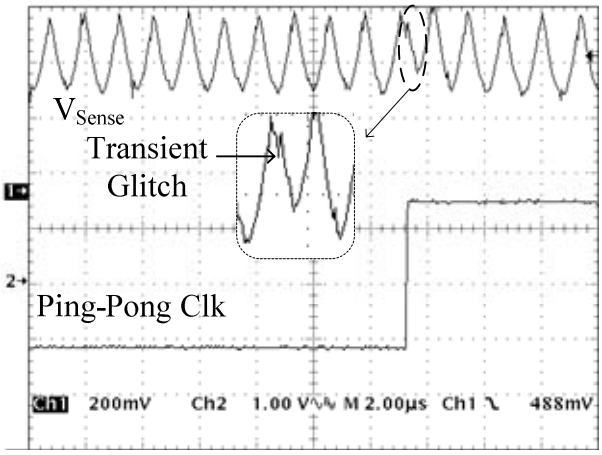


Figure 7.5—Worst-case transient glitch at the output of ping-pong g_m-C filter.

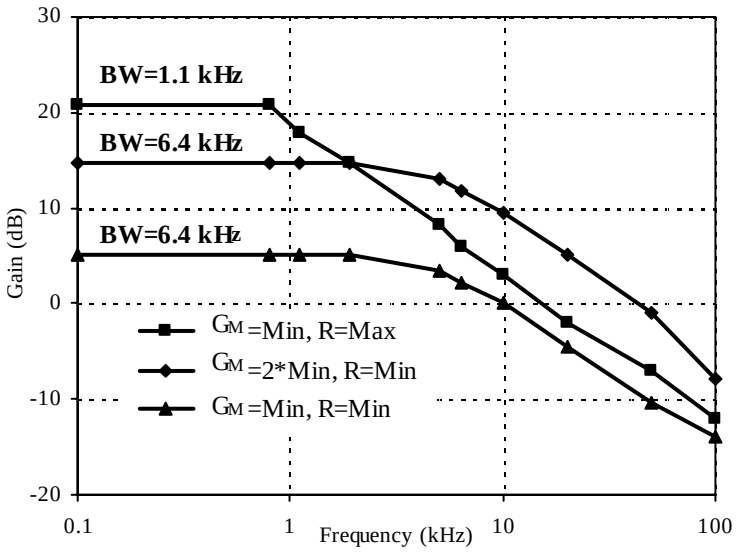


Figure 7.6—Measured frequency response of g_m-C filter.

The turning and calibration ranges were tested using different setups. To test the tuning range, a 200 kHz, 50% pulse was placed at the input of the g_m-C filter, with magnitude varying from 60 mV to 340 mV which imitated inductors from 3 µH to 17 µH (i.e., $L = V_{Mag}\Delta T/\Delta I_{Test}$, where $\Delta T = 2.5$ µs and $\Delta I_{Test} = 50$ mA), while the g_m-C filter

output was monitored for tuning and tuning comparator output. When the tuning circuit was locked, the triangular peak-to-peak voltage of the g_m-C filter was compared to the 25 mV target value, and errors were calculated accordingly. For inductors ranging from 3.5 μH to 14 μH, the tuning circuit locks to the target gain setting with about -4% error (Figure 7.7). However, as the inductor goes out of range, the tuning circuit cannot lock to the target value, since the g_m-C filter reaches its maximum g_m when L goes below 3.5 μH and reaches its minimum g_m when L exceeds 14 μH. The error in the tuning circuit is less than the total AC error (i.e., -4% versus -9%), since tuning and switching frequencies are different (i.e., 200 kHz versus 780 kHz) and g_m-C filter frequency response deviates from its ideal single-pole response of -20 dB/dec because of parasitic poles, as shown in Figure 7.8. The bold line is the g_m-C filter high-frequency gain and the thin line is the ideal -20 dB/dec slope (test setup, g_m = min and R = max). While at 200 kHz, the ideal and measured gains coincide, at 800 kHz, the g_m-C filter is about 0.5 dB (5%) below the ideal gain, which explains the -5% discrepancy between the tuning loop and AC error.

Using a tuning frequency close to the switching frequency eliminates this error at the cost of higher-magnitude oscillations at phase node (V_{Ph}) when a triangular current is forced into the inductor at tuning. The higher oscillations can be damped using a smaller resistor, R_{Damp}, as discussed in Section 6.2.6, but in that case the portion of current flowing through R_{Damp} is no longer negligible, which reduces the accuracy.

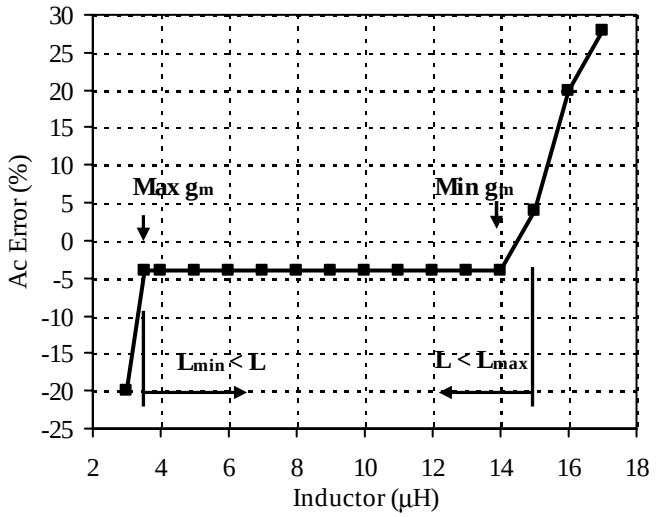


Figure 7.7—Tuning range: tuning AC error versus inductor value. The bold line is the g_m-C filter high-frequency gain and the thin line is the ideal -20 dB/dec slope.

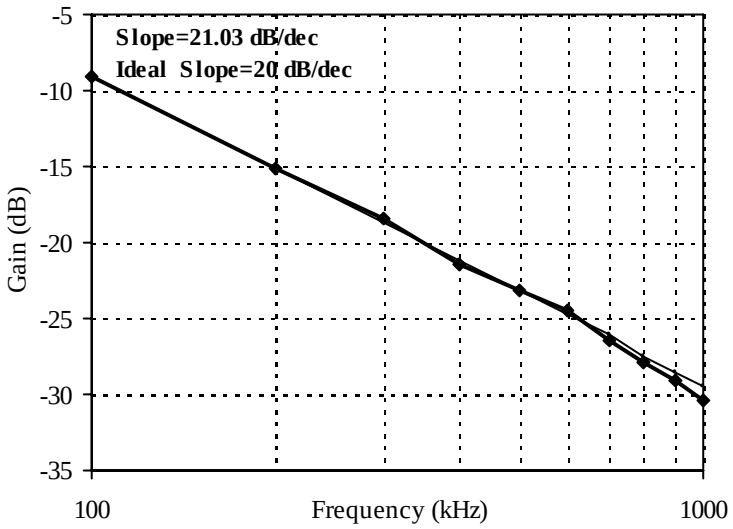


Figure 7.8—g_m-C filter high-frequency gain (g_m = min, R = max).

To check the calibration circuit performance and ESR range, constant DC voltages were placed at the input of the g_m-C filter to imitate the voltage across the inductor at start-up (i.e., $V_L = R_{ESR}I_{Test}$). Since tuning is performed before calibration, inductor range should be considered as well when considering ESR range. The calibration (DC) error is inversely proportional to the ESR value. In Figure 7.9, a filled inner area distinguishes the ESR-L range that results in low error (<5.5%) and an empty

outer area delineates the g_m-C filter programmability range. For ESR less than 48 mΩ (i.e., V_L = 2.4 mV), the calibration (DC) errors due to offsets are less than 5.4 %, but as ESR decreases to 44 mΩ and 26 mΩ, the errors increase rapidly to 12% and 27%, respectively (Figure 7.10), since the residual successive memorization (RSM) circuit goes out of range, and the g_m-C filter output is saturated in the offset measurement phase due to its high gain.

The input-referred offsets measured for various gains using the aforementioned method are illustrated in Figure 7.11. The minimum offset is 76 μV at a gain of 6.66. The input-referred offset is higher at low gains since charge-injection and clock feedthrough errors at the output are attenuated with low gains at the input. The input-referred offset increases at higher gains since the magnitude of amplified noise at the preamplifier output becomes so large that the preamplifier output is partly compressed. Therefore, averaging the capacitor output no longer compensates for random offset. It is expected that better offset performance is achieved by connecting the filter capacitor during calibration. The calibration circuit is less sensitive to input-referred offset for higher ESR values and DC calibration test current (Figure 7.12).

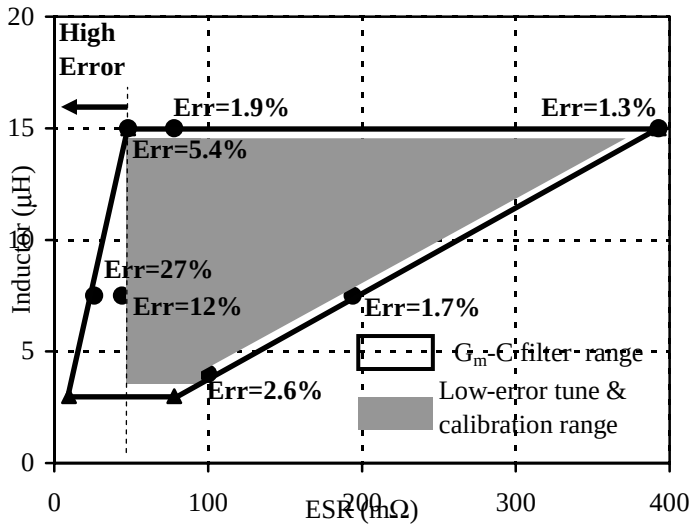


Figure 7.9—Calibration range: DC error versus ESR and inductor values.

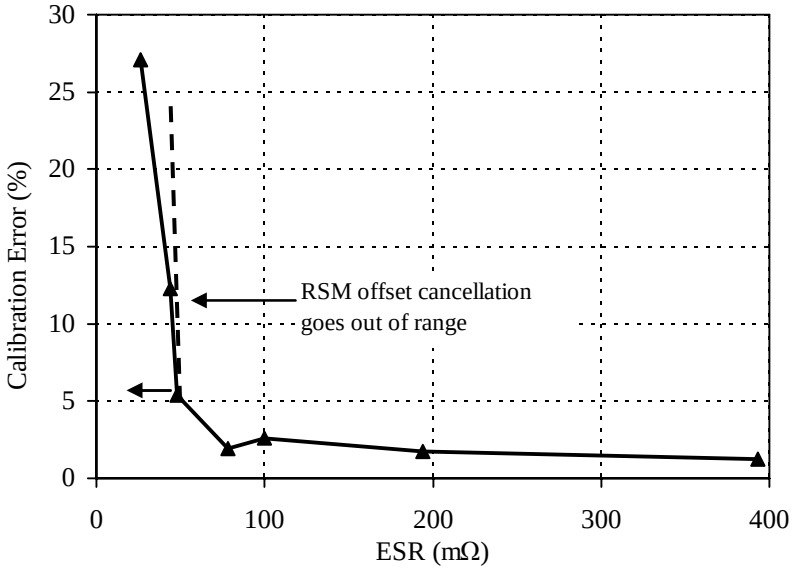


Figure 7.10—Calibration error versus ESR.

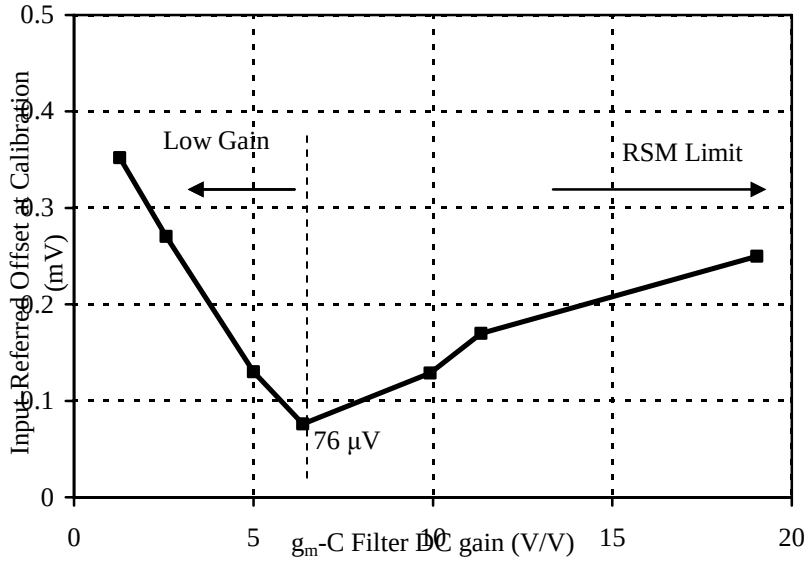


Figure 7.11—Calibration loop input-referred offset versus g_m-C filter gain.

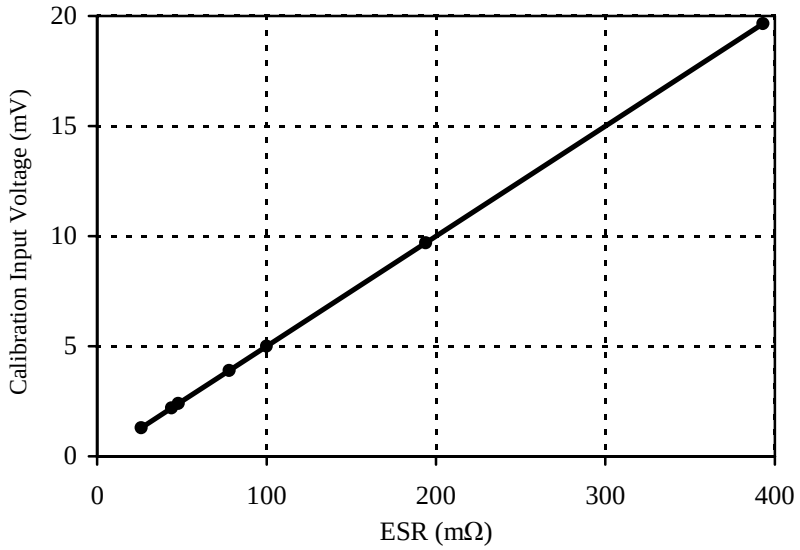


Figure 7.12—Calibration loop input voltage versus ESR value for 50 mA current.

The proposed current-sensing technique performance parameters are summarized in Table 7.1 along with specifications of the g_m-C filter. The proposed circuit is designed for 2.7 V to 4.2 V, and while individual blocks are functional in the whole range, the whole system was not tested beyond 3.5 V because of a problem in the design of the reference voltage. The total gain error of the circuit is evaluated by weighted addition of DC and AC errors. The total error is 8.51% for a test inductor of L = 3.9 μH and an ESR of 48 mΩ at a DC load current of 0.8 A and a ripple current of 0.2 A.

Table 7.1—Self-learning current-sensing circuit specifications based on experimental results.

Parameter	Value
Technology	CMOS 0.5 μm
Die Area (including pads)	3 mmx1.5 mm
Quiescent Current (normal operation, whole chip)	1.6 mA-2.1 mA (Various values of G_{M1})
Supply Voltage	2.6 V - 3.5 V
Self-Learning Circuit	
I_{Load}	0 - 0.8 A
$R_{gain}=V_{Sense}/I_L$	0.5 V/A
Error (I_{DC}=0.8 A, ΔI=0.2 A) ac DC (including offsets) Random Offset Systematic Offset (non linearity) Total (weighted DC + ac)	 -9% +8% ±0.4% -2% 8.51%
Tunable Inductor Range	3.5 μH -14 μH
Adjustable R_{ESR} Range	48 mΩ – 384 mΩ
Start-up Time (Worst Case)	384 ms
G_M-C Filter	
BW (1/RC) Programmability (Worst-case resolution by design)	1.1 kHz to 6.4 kHz (3.2%)
Gain (g_mR) Programmability (Worst-case resolution by design)	1.27 - 29.16 (V/V) (3.2%)
Input-Referred Offset (Gain=9.92, max R, three samples, V_{DD}: 3–4.2V, ICMR: 1 V - 1.5 V)	< ±210 μV
Transient Glitches	< 40 mV
Input-Referred Noise (C=60 pF, Gain=9.92, , max R)	93 μV
G_M-C Filter Nonlinearity ($\Delta g_m/g_m$) Rail-to-Rail V_{DD}=3 V	-57 dB
Second (Parasitic) Pole	4 MHz
Auto-zero clock frequency	1 kHz

The performance of the current-mode controller was also evaluated with both the proposed self-calibrating and sense resistor current-sensing techniques. Except for efficiency, both methods resulted in same performance, as was expected. The steady state output and switching node voltages of the buck DC-DC converter are illustrated in Figure 7.13. The output voltage ripple is less than 10 mV, ignoring the bounces at switching times. The bounces measured by the oscilloscope probe are due to ground

loops and parasitic inductances. The converter transient ripple is about 30 mV when load current changes from 0.1 A to 0.8 A instantaneously.

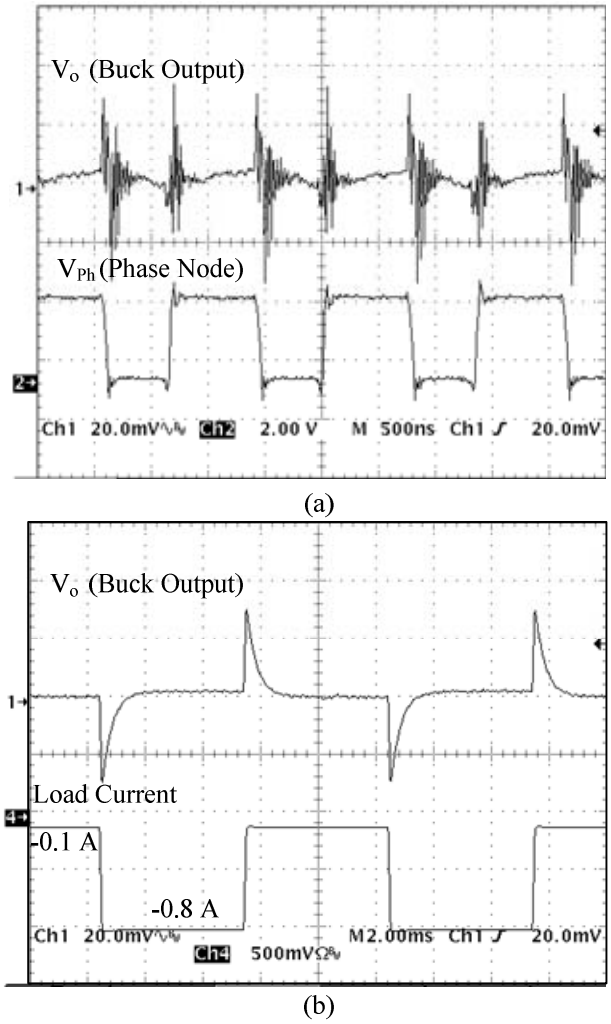


Figure 7.13—Buck converter output voltage ripple (a) Steady-state and (b) transient load.

The start-up waveforms of the buck converter are shown in Figure 7.14, which shows that the supply current is limited to 100 mA at the start-up (no output load). The buck converter output voltage versus DC load current is shown in Figure 7.15, where load regulation is limited to -0.34% because the current-mode controller employs a zero-frequency pole (i.e., integrator compensation).

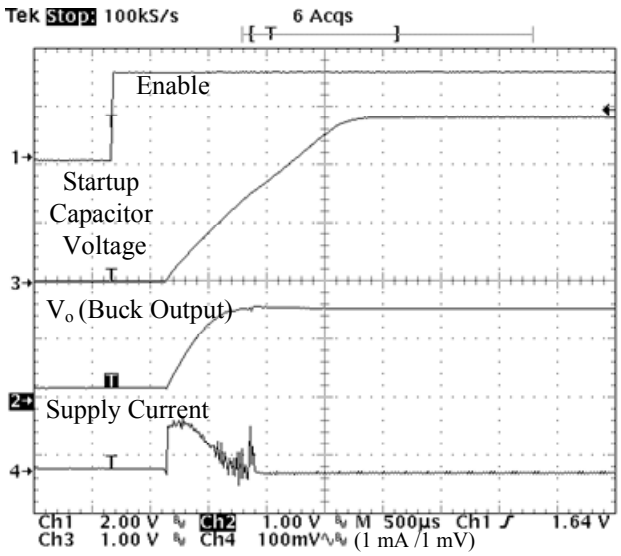


Figure 7.14—Buck converter start-up waveforms (no load at output).

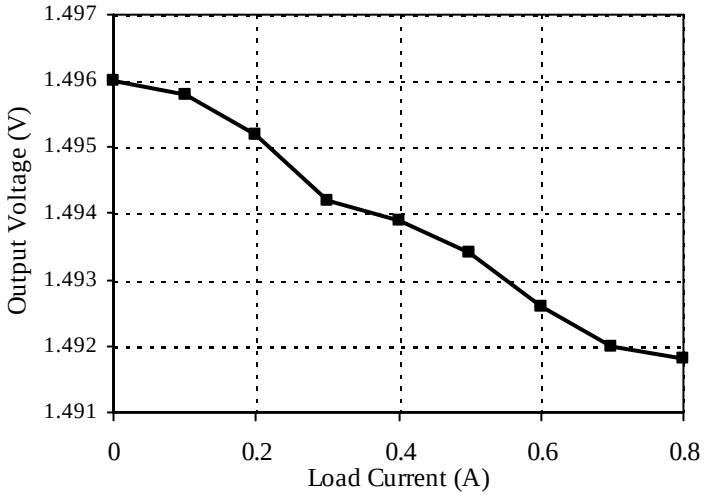


Figure 7.15—Buck converter output voltage as a function of output load current.

The effect of the current-sensing technique on efficiency is shown in Figure 7.16 for current loads from 0 A to 0.8 A. To measure the efficiency of the proposed current-sensing technique, the 50 mΩ reference sense resistor was shorted. To measure the efficiency of the R_{Sense} technique, the g_m-C filter was disabled and the output of the sense resistor differential amplifier was connected to the summing comparator "In1+" input into the current-mode controller. Figure 7.16 shows an efficiency increase ranging from 3.9% at 0.1 A to 2.6% at 0.8 A. The efficiency is low at low-load currents since a

constant-frequency PWM controller is used, and switching losses dominate at these loads. Efficiency is maximum around 0.5 A and gradually declines as load current increases becasue conduction losses in power MOSFETs “on” resistances. The current-mode controller key performance parameters based on experimental measurements are listed in Table 7.2.

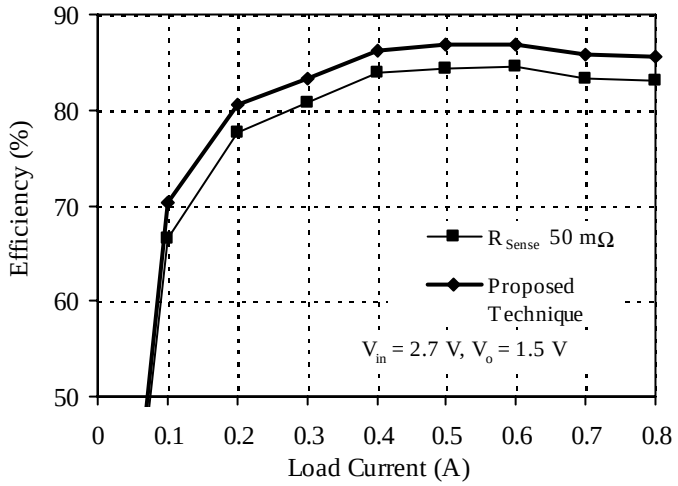


Figure 7.16—Comparison of buck converter efficiency using the proposed self-calibrating and R_{Sense} techniques.

Table 7.2—Current-mode controller specifications based on experimental results.

Parameter	Value
Controller Type	PWM Synchronous, Current Mode
Input Voltage	2.6 V to 3.5 V
Output Voltage (targeted for 1.5 V)	1.496 V
Output Current	0 ro 0.8 A
Switching Frequency	780 kHz
Output Voltage Ripple Steady State + Transient (0.1 A to 0.8 A)	<± 40 mV
Efficiency (0.8 A load, 2.7 V input) with Lossless Current Sensing with R_{Sense} Current Sensing	85.67% 83.05%
Load Regulation (LDR) (I_{Load} = 0 to 0.8 A)	-0.34%
Line Regulation (LNR) (V_{DD} = 2.7 V to 3.5 V)	0.85%
Soft Start Delay	2.2 ms

7.4. Issues and Fixes

Although the circuit was fully functional, two issues were encountered that limit the performance of the fabricated chip, and they should be resolved in future fabrications. These issues are higher–than-expected noise at the output of the g_m-C filter during calibration and instability of voltage reference network for high supply voltages.

Calibration Noise

The filter output capacitor is disconnected at calibration to increase speed, which increases filter bandwidth and equivalent output noise significantly. To verify the problem and characterize the calibration loop, the output of the comparator was disconnected from the digital core and additional off-chip circuitry was placed between the output of calibration comparator and input of digital core "Cal_stop" (Figure 7.17). The off-chip circuit compares the DC value of internal comparator V_{Comp} with half of the supply rail. If there is no noise, the internal comparator output is either zero or one, but because of thermal noise, when V_{Preamp} becomes close to V_{Cal}, its output is a stream of zeros and ones. However, its average can be used to measure the offset-cancellation performance of the calibration loop. Since the noise is random, when the loop settles at the target gain (i.e., $(g_mR).20.R_{ESR}I_{Test} = V_{Cal}$) internal comparator DC output is at half of the rail. Therefore, an external comparator is used to compare the internal comparator output with $V_{DD}/2$ and to control the calibration counter.

To measure the calibration offset, the calibration loop was run for a known input voltage until the loop was locked (i.e., the calibration loop had stopped) and the calibration gain at the locked position was measured (i.e., g_mR). Consequently, the input-referred offset of the loop can be determined as

$$V_{off} = \frac{(20(g_mR)V_{in}) - V_{Cal}}{20(g_mR)}, \qquad (7.1)$$

where V_{Cal} is the calibration target voltage (0.5 V) and V_{in} is the input DC voltage to the g_m-C filter at calibration. The measurement can also be done open loop, by setting the filter gain and changing the input voltage until the external comparator output becomes $V_{DD}/2$.

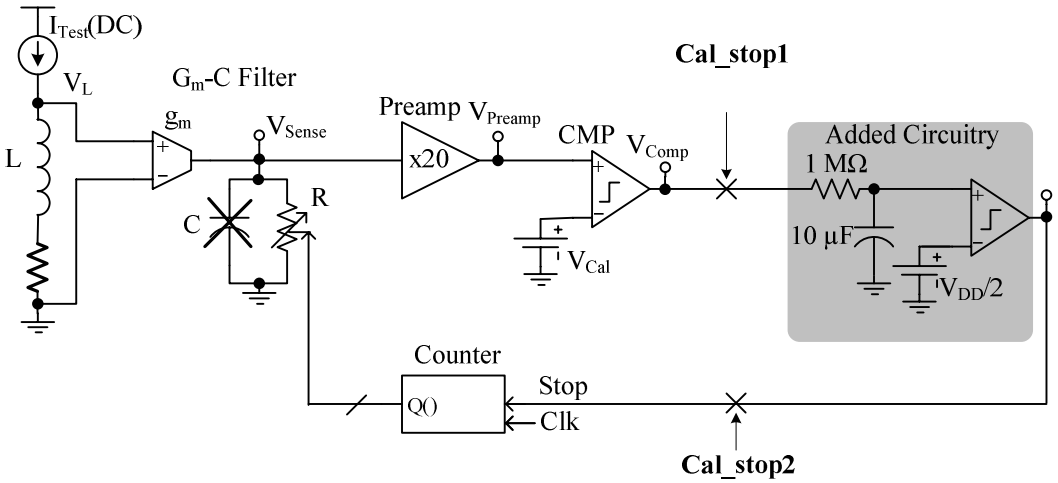


Figure 7.17—Disconnecting output filter capacitor at the calibration phase increases its bandwidth and noise and reduces calibration accuracy. The off-chip filter and comparator are placed to bypass the problem.

The root cause of the issue (noise) was confirmed with the external circuit and oscilloscope average waveforms of the g_m-C filter and preamplifier output g_m-C filter at calibration. To address this issue, two modifications are proposed as are illustrated in Figure 7.18 and are as follows:

1. The g_m-C filter capacitor should be connected back to the filter output during calibration.
2. A digital low-pass filter should be added for additional noise removal. The digital filter looks at multiple samples from the calibration-loop comparator instead of only a single sample to trigger Cal_stop. This filter can be implemented with a 4-bit counter and an RS latch. The counter clock frequency is 64 times the SW1 clock frequency. Therefore, the counter waits for 16 events out of possible 32 sampling events to release a calibration stop, preventing a false calibration stop because of the noise.

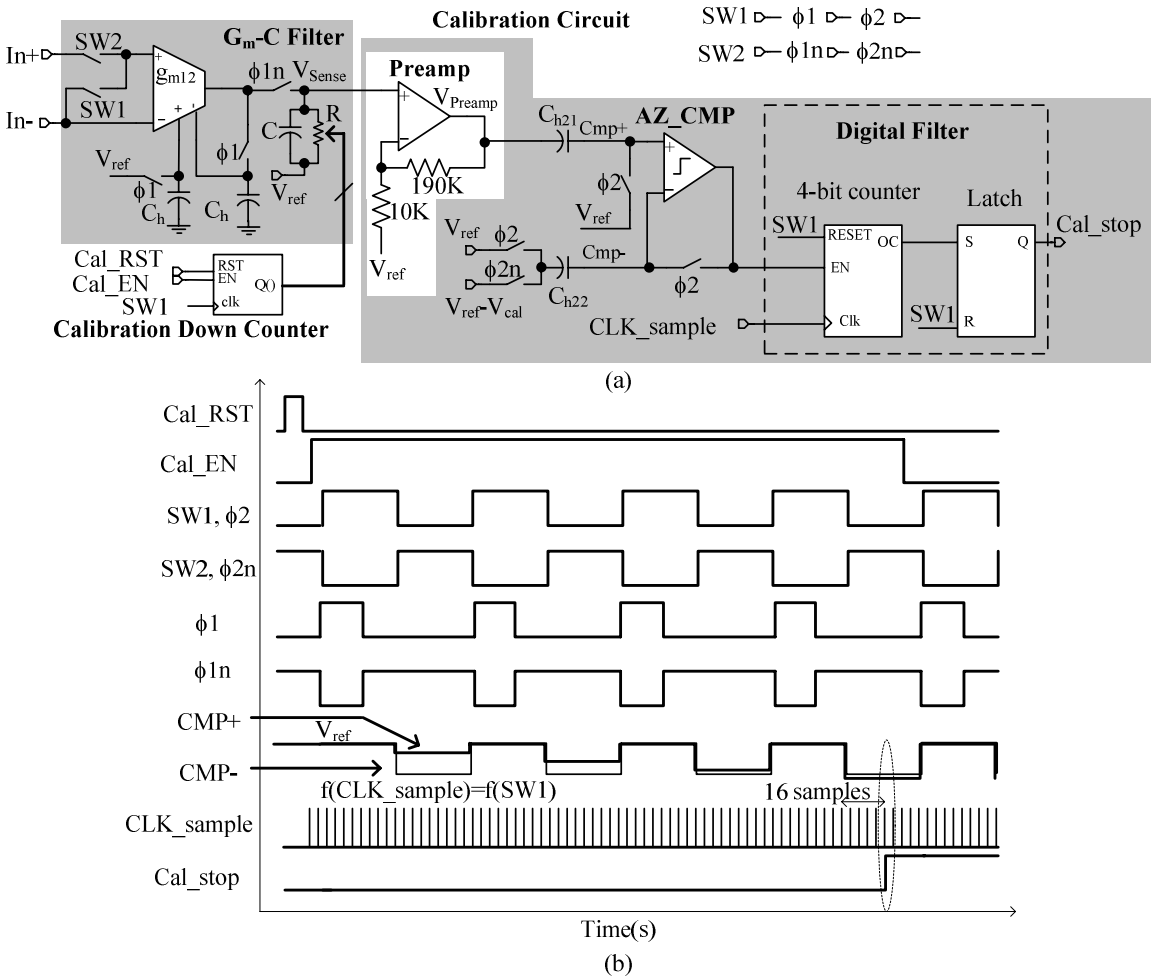


Figure 7.18— Modified calibration circuit to address the noise issue (a) circuit implementation with filter capacitor and a digital low-pass filter and (b) corresponding waveforms.

Reference Instability

Another issue encounter in final chip was the instability of the voltage reference and current-biasing circuit for supply voltages V_{DD}>3.5 V. The root cause of this issue is the improper placement of the compensation capacitor in the reference circuit. Instead of compensating the two-stage reference amplifier A_{ref} with miller capacitor, the circuit is compensated with a capacitor at the relatively low impedance point V_{ref}(1 V) using a large capacitor (Figure 7.19). The reference oscillations were damped for V_{DD}<3.5 V using large capacitors at input V_{refin}, and across off-chip resistor R_c. This phenomenon can be considered a conditional instability since it was not caught with AC and transient simulations. If the supply voltage is high enough, the transistors N1 and N2 operate in

saturation and a high gain path exists from gate to drain. Therefore, if there is a noise on the gate of these transistors, it will be amplified and results in large-signal cycles on the drains of N1 and N2. However, if supply voltage is low, these transistors are in triode, and therefore the oscillations are damped. The chip-level fix is to compensate the reference block by using a Miller capacitor inside $A_{ref,}$ and cutting the V_{ref} (1 V) connection to the pin. It should be mentioned that since a different reference scheme was used for test chips with individual blocks on them, the problem was not observed in those chips and therefore various blocks such as g_m-C filter, calibration loop and error amplifier could be characterized in the whole supply range. Table 7.3 lists the final chip issues and their proposed fixes.

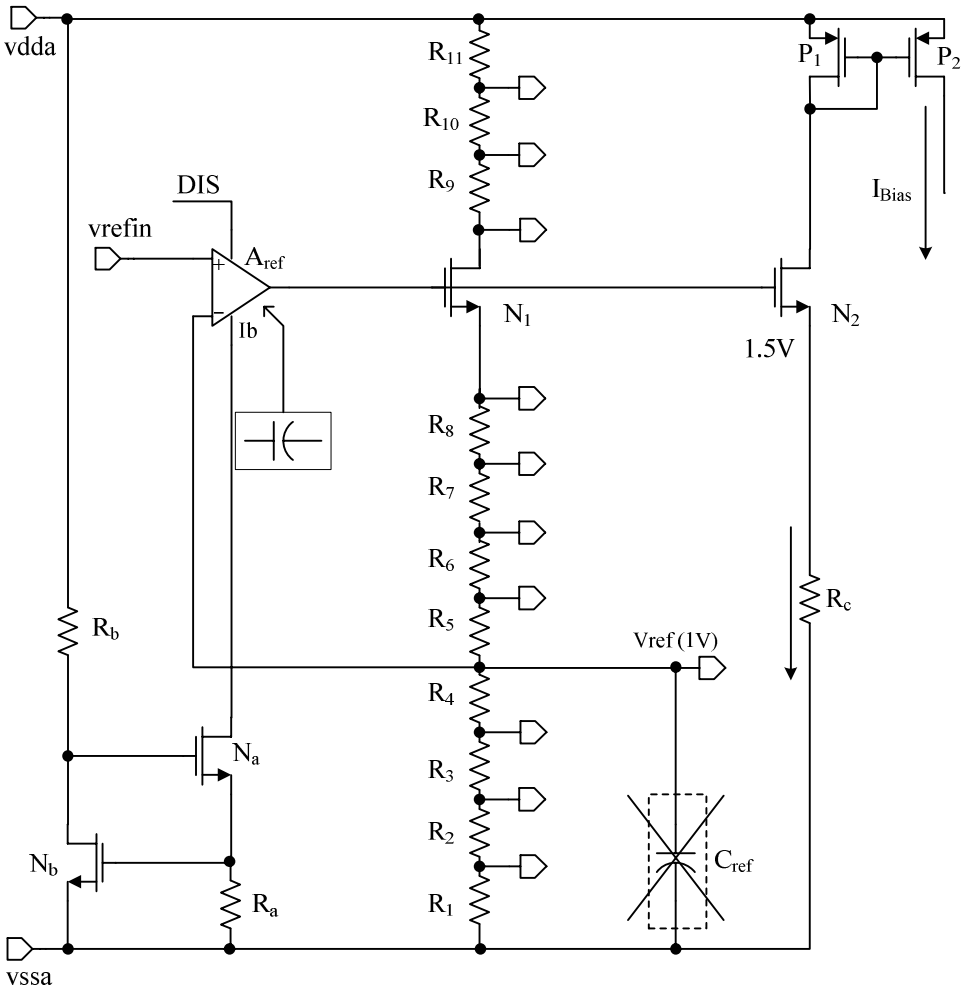


Figure 7.19—Relocating the compensation capacitor in the reference voltage network from output pin to inside amplifier A_{ref} to fix reference instability issue.

Table 7.3—Table of final chip issues and their proposed fixes.

Issue	Description	Proposed Fix
Calibration Noise	Removal of filter capacitor C of g_m-C filter at calibration to shorten the calibration time increases the noise due to high filter bandwidth, and reduces the calibration loop accuracy.	1. Connect capacitor C during calibration. 2. Add a digital low-pass filter to calibration loop.
Reference Instability	For V_{DD}>3.5 V, the reference becomes unstable because of improper location of compensation capacitor.	Relocate the reference compensation capacitor.

SUMMARY

The characterization and debugging of the proposed current-sensing IC prototype and its test bed, the buck current-mode-controlled switching regulator, were discussed in this chapter. Except for additional noise in the calibration loop, which was addressed in measurements with some off-chip circuitry, and reference instability at voltages higher that 3.5 V, the proposed chip achieved the target and simulation performance. The measurement results for the proposed current-sensing IC prototype achieved overall DC and AC gain errors of 8% and 9%, respectively, at 0.8 A DC load and 0.2 A ripple currents for inductors from 4 μH to 14 μH and ESR from 48 mΩ to 384 mΩ when lossless, state-of-the-art lossless schemes achieve 20% to 40% error and only when the nominal specifications of the power stage (power MOSFET or inductor) are known. Moreover, the proposed circuit improves the efficiency of the implemented buck converter by at least 2.3% over the traditional sense resistor technique with a 50 mΩ sense resistor.

CHAPTER 8

CONCLUSIONS

Based on the literature survey, proposed technique, and experimental evaluation of the various prototypes built, several conclusions and projections can be formulated. This chapter reviews the fundamental problem of current-sensing in power supplies and summarizes the system- and circuit-level solutions that were developed to address the various issues, followed by a comparison of the proposed technique to state-of-the-art solutions. The chapter concludes with recommendations on further work, the application of the proposed current-sensing technique in state-of-the-art systems, and how this research fits and conforms to the general trend of future high-performance analog circuits.

8.1. Contributions

The main objective of this work was to develop an on-chip, lossless, and accurate current-sensing technique for switching regulators. As discussed in detail in Chapter 2, the motivating force of this research are advanced current-dependent control techniques for integrating large power inductors and bulk capacitors, improving efficiency, optimizing transient response, and reducing the cost of high-performance switching regulators for next-generation portable devices such as cellular phones, digital cameras, and PDAs. None of these advanced techniques can be realized without an integrable, lossless, and accurate current-sensing circuit that measures the inductor current and therefore the output current, and none of the available current-sensing techniques is accurate if implemented on-chip.

Theoretically, lossless current-sensing circuits must only sense voltages because sensing current implies additional series devices, and therefore, power losses. Measuring the current flowing through an existing device from voltage information only requires knowledge of the device's impedance (i.e., series resistance, inductance, or capacitance). For a switching power supply, the inherent series path elements consists of an inductor, output capacitor, and power switches, which are normally off-chip and are selected by the end user, rather than the IC designer. Thus, the IC designer is not cognizant of these off-

chip components during the IC design cycle. The key contribution of this research is a method through which a power management IC measures off-chip component values during start-up and power-on-reset events in the process of adjusting an on-chip filter used to measure the current. The resulting contributions can be decomposed as follows.

Integrated, Lossless, and Accurate Current-Sensing Technique (Chapter 3)

The main contribution of this research is to introduce an integrated, lossless, and accurate current-sensing technique for DC-DC converters, whereas currently available techniques are either lossless or accurate but not lossless. The proposed technique is based on the lossless and precise (i.e., low noise), but inaccurate, filter technique, in which a filter processes the voltage across the inductor (Section 2.2). The proposed technique introduces tuning and calibration phases at start-up to adjust DC gain and bandwidth of on-chip filter DC gain and bandwidth to the off-chip inductor cut-off frequency and ESR and consequently enhances accuracy. The proposed technique was verified experimentally with a 0.5 μm CMOS process. Although the proposed current-sensing technique was developed and applied to a buck DC-DC converter, its application can easily be extended to other power circuits such as boost and buck-boost DC-DC converters, as well as AC-DC and DC-AC converters.

Another contribution of this research is the self-calibration feature for the current-sensing circuit. In contrast to other techniques, the proposed technique maintains accuracy for a wide range of inductors and ESR values. The range is determined by the programming range of on-chip filter gain and bandwidth.

Methods to Match On-Chip Filters to Off-Chip Inductors (Chapter 3)

Two methods of tuning and calibration, low and high frequency, were proposed to adjust and match an on-chip filter to an inductor (Chapter 3). In low frequency tuning, a sinusoidal test current is directed into the inductor. First, the bandwidth of current-sensing filter is adjusted to the inductor cut-off frequency by equating the phases of the input test signal and the filter output via a programmable resistor. Then, during calibration, a DC current is sourced into the inductor, and transconductance g_m is adjusted until the target gain is achieved.

In high frequency tuning, a triangular test current is sourced into the inductor, and the high frequency gain of the current-sensing filter is adjusted by monitoring the amplitude of the g_m-C filter's output and adjusting its transconductance value. Then, during calibration, a DC test current is directed into the inductor and the DC gain is calibrated to its target value by monitoring g_m-C filter output and varying a resistor value. In high frequency tuning and calibration, the filter's bandwidth is not directly adjusted to inductor's bandwidth, but gain-bandwidth product are set, which achieves the same result. The low and high frequency tuning and calibration methods were verified with a discrete PCB and an integrated circuit in AMI's 0.5-μm CMOS process prototypes, respectively.

Method to Measure Inductance and ESR (Chapter 3)

Digital control is a recent research direction in the design of switching regulators [110]. The idea is to utilize the processing power of digital-signal processors (DSPs) to alter the controller on-the-fly to achieve optimized efficiency and transient response. Nevertheless, all of the promising features of a digital controller depend on sensing power-stage's voltages and currents and identification [111] of external power devices such as power inductors and output capacitors. The open-loop version of the high frequency tuning technique can be used in a digital controller to ascertain the inductor value. The same applies to the open-loop version of the calibration technique to ascertain inductor ESR, but its value may not be as useful as inductor value in control of DC-DC converters.

Continuous Low-Offset, Low-Glitch, Programmable Gain and Bandwidth CMOS g_m-C Filter (Chapter 6.2.1)

A continuous low-offset, low-glitch, programmable gain and bandwidth g_m-C filter (Chapter 6.2.1) was developed, designed, and built to meet the challenging specifications of the current-sensing filter. The filter was implemented in an AMI's 0.5-μm process and experimentally verified in the lab. To achieve continuous low-offset operation, ping-pong auto-zeroing techniques were used. A current-conveyor based g_m-cell was also proposed to meet the rail-to-rail input range and linearity requirements of the current-sensing circuit. Experimental results verified that less than ±210 μV of offset

were achievable for supply range of 3 V to 4.2 V, which is compatible with Li-Ion batteries and input common-mode range of 1 V to 1.5 V. The bandwidth is adjustable from 1.1 kHz to 6.4 kHz and the DC gain is variable from 1.27 V/V to 29.16 V/V with a resolution better than 3.2%. Output-referred "Hand-over" glitches are also reduced and limited to less than 40 mV because the ping-pong operation occurs at the dominant pole-setting node, where a large capacitor resides.

Low-Power and Accurate CMOS Ramp Generator for Control of Switching Regulators (Chapter 6.2.6)

Ramp- and pulse-signal generators are critical in controlling the frequency and duty-cycle of pulse-width modulated (PWM) switching supplies. They are normally implemented with a current source that charges a capacitor and a reset switch that discharges the capacitor. The timing of the charging and discharging sequence is controlled by two comparators, whose reference signals set the lower and upper limits of the ramp. A continuous fast, and consequently high-powered, comparator is required to ensure that the reset operation is short and prevent large errors in amplitude and frequency of the ramp signal. To alleviate the comparator's bandwidth and power requirements, a scheme was proposed by which the circuit generates asymmetric triangular signal to imitate the ideal ramp only until 90% of the period, leaving more time for the switch and its controlling comparator to reset the ramp accurately before the onset of the following switching cycle (Chapter 6.2.6). A lower propagation delay requirement reduces design complexity, power consumption, and silicon real estate. The proposed 0.5-µm CMOS design uses 256 µA quiescent current and its amplitude errors are limited to 30 mV at 800 kHz operation.

Fast and Reliable Method for Verifying Top-Level Simulation of Complex Mixed-Signal Switching Regulator ICs (Appendix A)

Some other contributions of this research occurred during the execution stages. The most significant execution-stage contribution happened during top-level simulations of the current-mode controller. A top-level, transistor-based simulation of a complex mixed-signal system is a critical step in the verification phase cycle of integrated circuits (ICs). It is normally performed just before fabrication and unfortunately imposes

cumbersome bottlenecks in the design flow. It consumes so much time, in fact, that proper functional verification is not always viable, since each simulation can take up to a day. Switching power supplies fall under this category, because of their highly complex and heavily interconnected analog and digital switching components, surrendering to convergence issues and increasingly long computational times. Verification is, by nature, an iterative process, whereby each problem found requires another simulation to ensure a proper fix is in place. Because of the complexity of a large system, minor errors can cost days, increasing design time and time-to-market. To overcome this problem, a top-level simulation strategy with minimal time overhead was proposed to increase the reliability of top-level, transistor-based systems. An optimized sub-block replacement sequence for switching regulators was determined through case-study analysis of a PWM current-mode controller, in which the ramp- and digital-signal generator and drivers were found to incur 60% of the simulation time while the amplifier, comparator, and reference only consumed 11%. Thus, analog blocks were put at the top of the replacement list and their digital counterparts at the bottom. The proposed top-level simulation strategy is discussed in detail in Appendix A.

Table 8.1 summarizes the main contributions of this work. Table 8.2 lists the published and submitted papers based on this research.

Table 8.1—Summary of contributions.

No.	Description
	System-Level Contributions
1	Integrated, lossless, and accurate current-sensing technique - the inductor, itself, used as the current-sensing element - integrated version of filter technique - combined lossless and accurate operation
2	Self-calibrating current-sensing technique - user friendly (i.e., the user need not design or alter an off-chip element to obtain accuracy)
3	Low-frequency tuning and calibration method to adjust the on-chip filter to off-chip inductor
4	High-frequency tuning and calibration method to adjust the on-chip filter to off-chip inductor
5	Method for measuring off-chip power inductor value
	Circuit-Level Contributions
6	Continuous low-offset, low-glitch, programmable gain and bandwidth g_m-C filter
7	Highly linear, rail-to-rail input transconductance cell
8	Low-power and accurate ramp generator for switching regulators
	Execution Contributions
9	Method for fast top-level simulation of switching regulators

Table 8.2—List of published and submitted papers.

No.	Description
	Published
1	M. Gildersleeve, H.P. Forghani-zadeh, and G.A. Rincón-Mora, "A comprehensive power analysis and a highly efficient, mode-hopping DC-DC converter," in *Proc. 2002 Asian-Pacific Conference on ASICs*, pp. 153-156.
2	H.P. Forghani-zadeh and G.A. Rincón-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. 2002 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 577-580
3	H.P. Forghani-zadeh and G.A. Rincón-Mora, "A lossless, accurate, self-calibrating current-sensing technique for DC-DC converters," in *Proc. 2005 Industrial Electronics Conference (IECON)*, pp. 549-554.
4	H.P. Forghani-zadeh and G.A. Rincón-Mora, "A continuous, low-glitch, low-offset, programmable gain and bandwidth g_m-C filter," in *Proc. 2005 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1629-1632.
5	E. Torres, L. Milner, N. Keskar, M. Chen, H. Pan, V. Gupta, P. Forghani, and G.A. Rincón-Mora, "SiP integration of intelligent, adaptive, self-sustaining power management solutions for portable applications," *in Proc. IEEE 2006 International Symposium on Circuits and Systems (ISCAS)*, May 21-24, 2006.
	Submitted
6	H.P. Forghani-zadeh and G.A. Rincón-Mora, "1.8 V, 770 kHz, 0.5 µm CMOS ramp generator circuit for DC-DC converters," submitted to *Electronics Letters*.
7	H.P. Forghani-Zadeh and G.A. Rincón-Mora, "A strategy for fast and reliable top-level simulation and verification of mixed-signal DC-DC converter ICs," submitted to *IEE Proceedings on Circuits, Systems, and Devices*.
8	H.P. Forghani-zadeh and G.A. Rincón-Mora, "A 210 µV offset, continuous, 40 mV glitch, highly linear, rail-to-rail input, programmable gain and bandwidth g_m-C filter," submitted to *IEEE Transactions on Circuits and Systems I (TCAS-I).*
9	H.P. Forghani-zadeh and G.A. Rincón-Mora, "A self-learning, accurate, and lossless current-sensing technique applied to a current-mode controller," to be submitted to *IEEE Journal of Solid-State Circuits (JSSC).*
	Trade Articles
10	G.A. Rincón-Mora and H.P. Forghani-zadeh, "Accurate and Lossless Current-Sensing Techniques: A Practical Myth?" Power Management Design Line (PMDL) (http://www.powermanagementdesignline.com), March 17, 2005.
11	G.A. Rincón-Mora and H.P. Forghani-zadeh, "Self-learning switching DC-DC converters meet smart power," Power Management Design Line (PMDL) (http://www.powermanagementdesignline.com), October 13, 2005.
12	G.A. Rincón-Mora and H.P. Forghani-zadeh, "Simulating Top-Level DC-DC Converter Circuits Fast," Power Management Design Line (PMDL) (http://www.powermanagementdesignline.com), April 15, 2006.

8.2. Comparison to State-of-the Art

By nature, designing electronic systems and circuits involves making trade-offs. There is no circuit topology that is perfect, and each one has its own advantages and drawbacks. This subsection compares features of the proposed current-sensing technique with popular state-of-the art techniques: sense resistor, MOSFET R_{DS}, Sense-FET, and filter techniques.

8.2.1. Advantages

The proposed technique is lossless, unlike the traditional sense-resistor technique, since it does not require a sensing element to be inserted in a high current path. Moreover, the proposed technique overcomes the inherent inaccuracies of available lossless techniques by introducing tuning and calibration to adjust an on-chip filter to an off-chip inductor during start-up. As a result, the proposed integrated circuit is accurate for a range of inductors from which the end-user is free to choose, while state-of-the-art available lossless techniques are not accurate if integrated.

The lossless MOSFET R_{DS} technique, for instance, estimates the current from the drain-source voltage of a MOSFET switch, and its accuracy is therefore linked to the on-resistance value of the MOSFET, which varies significantly with temperature, process, and supply voltage (e.g., ±75%).

In the case of the quasi-lossless sense-FET technique, a mirror transistor is used to source a fraction of the switch current, and its accuracy relies on the matching performance of the current mirror, whose mirroring ratio is on the order of 1,000 and its operating region is in triode (i.e., Ohmic or non-saturated). Although accuracies of ±4% are reported [112], the mismatch and process variations cause errors as large as ±20% (3σ spreads), a result of the large device-size spread between the sense-FET and the power-FET in the mirror [113].

The lossless filter technique measures the inductor current by applying a low-pass filter across the inductor [114]. Nevertheless, its accuracy is dependent on the inductance, and matching a filter to the inductance is critical. Even when the inductance is known and the filter is well matched, component tolerances and operating-point variations can cause up to ±28% error (±15% initial inductor tolerance, ±11% ESR variance, and a

temperature range of 70°C) [114]. In practice, worse accuracies are expected to occur in applications with a wide temperature range (e.g., the commercial range for power supply chips is from -10 to 125 °C, and the error is around ±60%; see Chapter 4).

Similar to filter technique, the proposed technique is continuous and low-noise. MOSFET R_{DS} and sense-FET techniques are based on measuring current flowing into the power switches, which only conduct in a fraction of a period, rather than the current flowing into the inductor, which is continuous. In addition to discontinuity, measuring the current in power switches includes transient gate current. These transient gate currents can manifest themselves as large switching noises at the output of MOSFET R_{DS} and sense-FET current-sensing circuits, and therefore, limit their use in control applications such as current-mode controllers, where low-noise circuits are required.

8.2.2. Drawbacks

The main drawback of the proposed technique is its complexity. The g_m-C filter, tuning loop, calibration circuit, test-current converter, and triangular generator are the key building blocks of the proposed technique. Among these, the design of g_m-C filter and calibration circuits can be challenging due to their high-performance requirements, such as low-offset and high linearity. While the prototype circuit was deliberately specified to be stringent investigate all the problems and issues associated with the proposed technique, some of the specifications can be relaxed, depending on the demands of the application. For example, if higher test currents can be provided at start-up, higher offset levels can be tolerated. If the application only requires accurate high-frequency gain as in inductor multipliers (Chapter 2), there is no need for the calibration loop, the low-offset feature of the g_m-C filter, or high linearity performance from g_m-cell, since systematic offsets do not affect ac accuracy.

On the other hand, it should be noted that state-of-the-art power-management circuits are more complex today than they were several years ago, and their implementation would not be possible without the close collaboration of several IC designers and extensive reuse of previously designed blocks. The self-calibrating nature of the proposed current-sensing technique makes it suitable for reuse in most switching regulatos, and therefore the proposed current-sensing technique complexity of the

proposed research may be offset by technical merits especially with the context of reuse. A summary of how the proposed current-sensing technique compares with the state-of-the-art methods is offered in Table 8.3.

Table 8.3—Comparison of the proposed system with the state of the art current-sensing techniques.

Technique	R_{sense}	**MOSFET R_{on}**	**Sense-FET**	**Filter**	**Proposed**
Sense-Element Loss	50 mW	0	5 mW	0	0
Processing-Circuit Loss (1)(2)	0.5 mW	0.5 mW	0.5 mW	5 mW	5-10 mW(5)
Error	<±5%(3)	±75%(4)	±20%(4)	±60%(4)	±9%(6)
Advantages (1)	- Simple - Accurate	- Low Power - Integrated	- Simple - Integrated	- Low Noise - Continuous	- Low Noise - Continuous - Integrated - Accurate - Self Calibrating - User Friendly
Disadvantages (1)	- Lossy	- Very Low Accuracy - High Noise -Discontinuous	- On-Chip Switches - High Noise - Discontinuous	- Off-Chip	- Complexity - Designer-Unfriendly
Conditions	50 mΩ resistor		Mirror Ratio = 1/1000		I_{cc}(max) = 2 mA

(1) Assumptions: power supply of 2.7 V to 5 V, 50 mΩ power MOSFET resistance, 50 mΩ inductor ESR, and maximum load current of 1 A. All current-sensing techniques are designed to achieve a 0.5 V/A trans-impedance.
(2) Power consumption estimate is based on the author's experience with analog circuits and AMI's 0.5 µm process. The power dissipation is calculated for the maximum power supply (5 V). The amplifier bandwidth is selected to be five times the switching frequency.
(3) Based on an off-chip, temperature-independent sense resistor.
(4) See Chapter 2.
(5) Processing circuit (i.e., g_m-C filter) power loss can be reduced significantly if the linearity specification is relaxed. The proposed circuit processing loss depends on the value of transconductance.
(6) See Chapter 7.

8.3. Recommendations

Several challenges encountered in the implementation of the proposed technique deserve more attention. First, the possibility of implementing the current-sensing filter with other filter topologies such as an active RC instead of a g_m-C filter should be evaluated within the concept of complexity.. The active RC implementation was ruled out in the early design stages because of the parasitic capacitance introduce by the programming switches used to change gain and bandwidth, which would significantly

limit the filter bandwidth. However, this may not be an issue in high-performance processes technologies with lower junction capacitance and higher poly-sheet resistivity. Also, research into implementing a variable filter capacitor C instead of a variable g_m-cell for AC-gain programmability may prove useful for reducing the complexity of the g_m-cell and filter. Second, methods that can lower the sensitivity of the calibration loop to offsets and noise should be investigated. Third, temperature-compensation circuits for ESR temperature effects can be explored further.

8.4. The Future

Fortunately, there are many applications that can exploit the results of this research. High-performance, state-of-the-art, portable applications such as laptops, cell phones, and PDAs demand smart DC-DC converter supplies to be adaptive, power efficient, and reliably accurate. While it is possible to control some of these DC-DC converter topologies with only output voltage information [9], current-mode controllers usually result in a simpler regulator transfer function, especially in the case of boost and buck-boost converters. Current-mode controllers consequently result in simpler compensation networks, which are stable for a wide range of power inductors and capacitors [9]. Moreover, every practical switching regulator includes an over-current detection circuit, which protects the system against over-current events. Apart from the historical use of inductor current for protection and control, recent applications have exploited current-sensing: in mode-hopping applications, it increases the power efficiency [115, 116]; in multiphase converters, it balances loads of power stages [117]; in single–inductor multiple-output regulator architectures [118], it provides control; and in inductor multipliers, it allows integration of the power inductor [119].

Nevertheless, when considering implementation of these advanced techniques, requiring current-sensing circuits proves to be a disadvantage and even a show-stopper because of the lack of an integrable, lossless, and accurate technique for DC-DC converters. The proposed current-sensing technique is a viable solution to address this problem. It should also be mentioned that the need for a high-performance current-sensing circuits is irrespective whether traditional analog or DSP-powered digital controllers rule the future of DC-DC controllers.

A comparison of the proposed technique with the trends for design of future high-performance analog circuits can be valuable, too. Several researchers studying the future of analog circuit design [120-123] predict the extensive use of calibration circuits (Figure 8.1(a)) to enhance the linearity and offset of analog circuits. Other researchers suggest parallel analog blocks (i.e., redundancy) along with calibration (Figure 8.1(b)) to achieve these goals. These trends are driven by the fact that while there is an inherent limit on the speed and noise performance of circuits for a given power dissipation in a process, there is no such limit on how much offset and linearity can be improved by calibration. The proposed self-calibrating circuit falls well into these trends, which significantly improves its viability of use in new coming state-of-the-art elections.

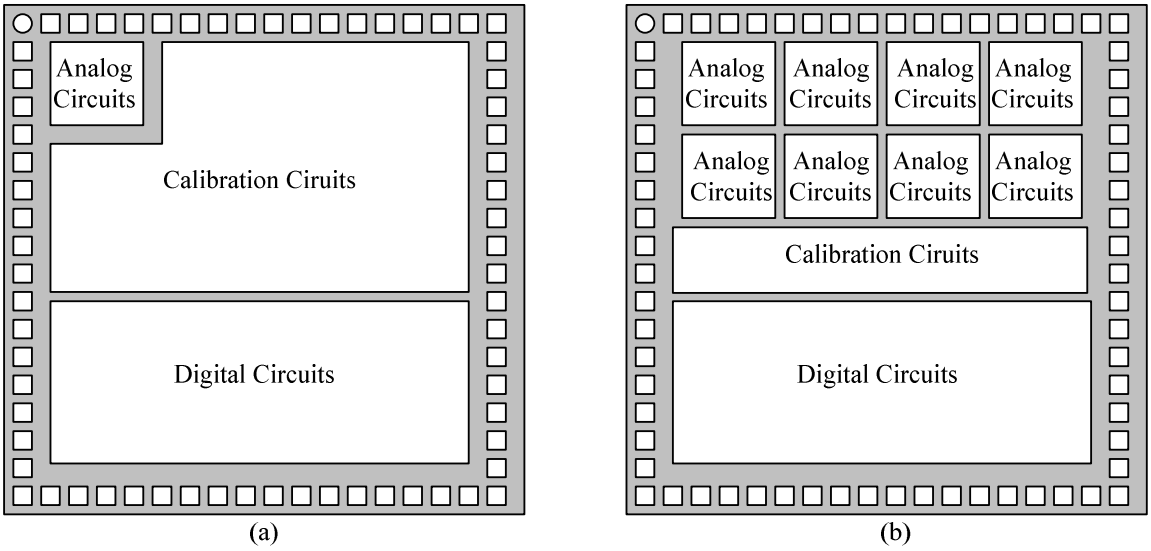


Figure 8.1—Research on the near-term future of analog ICs suggests a major part of die area of future analog ICs are dedicated to (a) extensive calibration or (b) parallel analog blocks (redundancy) along with calibration to achieve high performance [123].

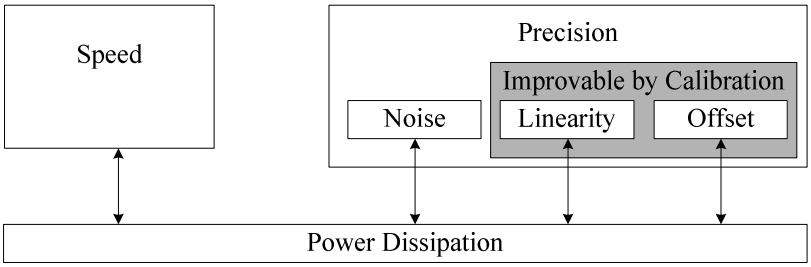


Figure 8.2—While there is an inherent limit on the speed and noise of circuits for a given power dissipation in a given process technology, there is not a theoretical limit on offset and linearity that can be improved by using calibration circuits [121].

APPENDIX A

A FAST AND RELIABLE TOP-LEVEL SIMULATION STRATEGY FOR MIXED-SIGNAL ICS AND ITS APPLICATION TO DC-DC CONVERTER CIRCUITS

A set of top-level transient simulations is usually necessary to verify the functionality of mixed-signal integrated circuits (ICs) just before fabrication. For highest fault coverage, all transistor-level simulations should be performed. Unfortunately, the simulation time for a complex system using all transistor-level models is many times prohibitively long, each simulation taking hours to days to complete. A switching DC-DC regulator constitutes one such mixed-signal example, with complex analog and high power switching digital circuits embedded onto a single substrate. The resulting simulation scenario demands the simulator to simultaneously resolve a vast number of equations at each step of a transient simulation run, which typically exceeds 1,000 switching cycles for start-up alone and incurs in the order of several hours to days of CPU time. As a result, considering the competitive time-to-market nature of the semiconductor industry, most designers concentrate their efforts on exhaustive, transistor-level, sub-block designs and opt for simple top-level simulations using a combination of transistor-based and behavioral models to *partially* verify inter-block connectivity and basic system functionality. That is to say, designers sacrifice top-level verification for time-to-market, which is not ideal and sometimes costly. Forfeiting better top-level simulations may mask interface and parasitic problems like inadvertent supply-to-ground resistive links, which translate to leakage currents. This problem is exacerbated with the growing demand for higher integration of system-on-chip (SoC) solutions. Sacrificing verification is difficult to justify when high yields are necessary to compete and turn a profit, which is why the need for quicker transistor-based top-level simulations is paramount.

The approach of state-of-the-art simulations for mixed-signal systems is to develop better behavioral models and partitioning circuits to analog and digital functional

blocks [124-132]. The models, unfortunately, lack the electrical details of parasitic junction diodes and diffusion resistors present in silicon-based electronics, the effects of which are seen during top-level system operation (e.g., leakage currents, unexpected loading events, oscillations, etc.). Literature on simulating specific types of circuits, like DC-DC switching converters [133-138], also focus on developing simplifying models, which are extremely useful in the system design phase, but relatively ineffective in the verification phase, where transistor-based models are necessary to identify parasitic electrical faults in the system.

This chapter proposes a top-level transient simulation strategy for mixed-signal circuits to minimize the verification time, or equivalently, maximize the fault coverage by using as much transistor-level models as possible in top-level simulations, while meeting verification-time deadlines. The proposed solution is to identify and delay replacement of transistor-based models of computationally extensive circuits, detecting most of the errors first, through relatively quick simulations.

A.1. Switching DC-DC Converters

A.1.1. Operation

Switching regulators are widely popular in consumer and military applications, especially the portable market because they convert variable voltages into stable, predictable, and suitable supplies without incurring significant power losses, and therefore increasing the battery life and requiring less heat sinks and board real estate [139-140]. The circuit accomplishes this by periodically storing magnetic energy into an inductor and later relinquishing it almost losslessly to the load and relevant output capacitor. The energy charge and transfer cycles of the scheme not only force the circuit to conduct high currents but also to switch periodically. This switching is complicated by the fact that the duty cycle must be regulated by an analog loop to ensure the output voltage is reliable and controlled.

Figure A.1 illustrates the schematic of a typical pulse-width modulated (PWM) current-mode buck (step down) switching DC-DC converter. The power train, which is comprised of high- and low-side power switches M_H and M_L, inductor L, and capacitor C, is responsible for storing and transferring energy from input supply V_{in} to load I_L.

Error amplifier EA, comparator CMP, signal generator, bandgap reference voltage, driver and dead time control (DTC), and current-sensing blocks constitute the analog control loop responsible for regulating the output voltage to a stable and predictable value [137-139]. In practice, power-on-reset, start-up, protection, and mode-changing circuits are also included for safety, reliability, and performance.

By alternately switching high- and low-side power devices M_H and M_L on and off, V_{ph} is switched from input supply V_{in} to ground, the average of which is reflected at the output as a result of the LC filter properties. Output voltage V_o is therefore the average of V_{ph}, which is in turn a function of how often high-side switch M_H is on, in other words, its duty-cycle D and V_{in} ($V_{out} = V_{in}D$). Modulating duty-cycle D to regulate V_o is accomplished by comparing V_o and the reference via the amplifier, consequently generating slow-moving control signal EA_{out}, which ultimately sets duty-cycle D when compared against the inductor current. The driver and dead-time control circuit is used to rapidly turn on and off large power transistors, while simultaneously avoiding momentary shoot-through events (i.e., high- and low-side switching shorts) [140-142]. As can be appreciated, the analog and switching complexities of this system are vast, when considering every sub-block is designed with numerous transistors, each of which introduce several nodes, parasitic elements, and non-linear semiconductor current-voltage relationships.

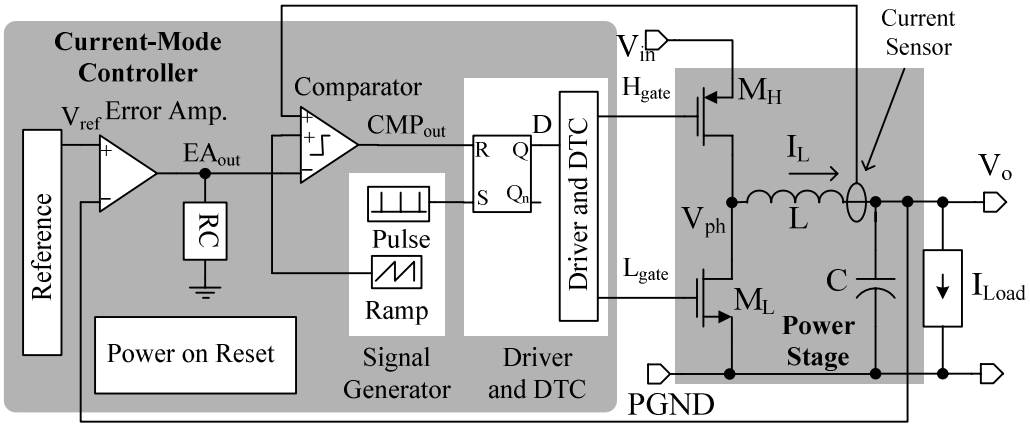


Figure A.1— A typical current-mode buck (step-down) pulse-width modulated (PWM) switching regulator circuit.

A.1.2. Macro Models

Accurate yet simple behavioral and functional models are not only important and useful in the system definition and design phases of mixed-signal circuits but also in the proposed top-level verification strategy. These macro models are typically implemented with a combination of high-level hardware description languages (e.g., VerilogA) and ideal electrical SPICE components [141-144] (e.g., independent and dependent voltage and current sources) under a Cadence platform, the same platform used for IC design, transistor-level simulations, and physical layout. Sharing the platform is important for seamless macro-to-transistor level transitions. For one thing, the top-level symbol of the macro-model can be designed to mimic that of the transistor-level block to minimize interconnectivity changes and maintain the integrity of the top-level schematic. Macro models should be comprehensive enough, having all input-output signals and enable-disable pins, to ensure the full system connectivity is truly tested

The power train, which is comprised of low- and high-side switches M_H and M_L, inductor L, and capacitor C (Figure A.1), is implemented with transistor-level models even when all other components use behavioral models because key DC-DC converter design specification parameters, such as power efficiency, output voltage ripple, load regulation, and transient response, are highly sensitive to the electrical characteristics of this stage. Parasitic components like the equivalent series resistors (ESRs) of the inductor and output capacitor are therefore included, to obtain accurate and reliable results. Purely analog circuits, such as the error amplifier, comparators, are modeled with ideal electrical SPICE components [144] and some Verilog-AMS blocks are added to model additional features such as enable-disable functions. Digital blocks such as RS latch, driver and dead-time control (DTC), and power on reset (POR) are mostly modeled with Verilog AMS [142, 143]. DC and time-variant sources are easily modeled with ideal SPICE dependent and independent sources.

A.2. Top-Level Verification Flow

A.2.1. Design Flow

Design flow typically starts after a market or research segment and application have been identified and defined, establishing specifications for a target system. A

suitable top-level system architecture is then designed and simulated using simple behaviorally based macro models, after which specifications for each macro model (i.e., sub-block) are generated. This part of the process constitutes the *system design* phase, illustrated in Figure A.2. At this point, transistor-level design, simulation, and verification of each sub-block against its specific target specifications are performed, both nominally and over process corners and temperature extremes. Since the simulations are relatively short, given the relatively low number of transistors used and the computing power of state-of-the-art computers, quasi-exhaustive verification is often achieved. Finally, before having the design fabricated (i.e., before *tape-out*), all the sub-blocks are interconnected and simulated together, which constitutes the transistor-based, top-level system. Verification is by nature an iterative process, however, whereby each problem found requires another simulation to ensure a proper fix is in place, and because of the complexity of a large system, minor errors can cost days, increasing design time and time-to-market.

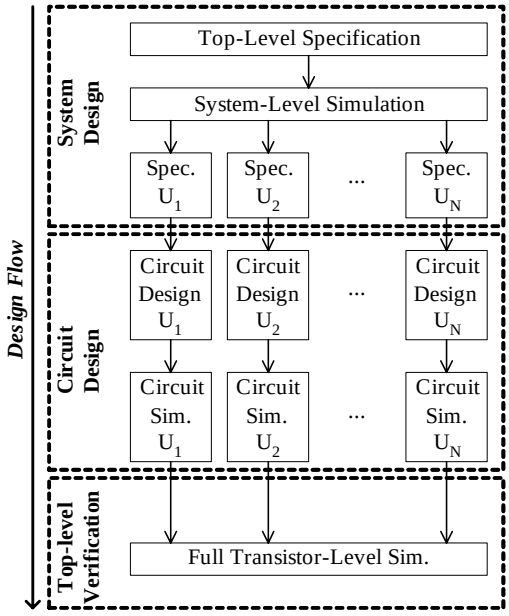


Figure A.2— Traditional design flow of electronic systems.

A.2.2. Proposed Top-Level Simulation Plan

The proposed strategy is to use the all behaviorally based macro-model simulation used in the system-design phase and selectively replace each sub-block, one at a time,

with its appropriate transistor-level circuit in the final verification phase, as shown in Figure A.3, gradually transitioning from an all macro-model to a full transistor-level simulation. The sub-blocks that are first substituted must be the least time-consuming circuits to simulate, consequently fully debugging and verifying connectivity and the system performance parameters associated with that specific sub-block. Substituting the next least time-consuming sub-block, and keeping the first one in place, accomplishes similar goals for the new block. The process continues until all of the blocks are fully replaced with their circuit-level models. A set of screening simulations are therefore developed to determine the optimal replacement order.

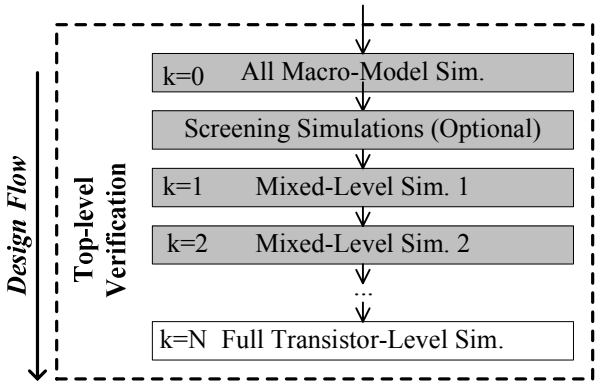


Figure A.3— Proposed top-level verification sequence of complex, mixed-signal systems.

The expected value of the simulation time of the proposed strategy, excluding the optional screening simulations, which are non-recurring in nature, is the summation of the various intermediate simulations,

$$E\left(t_{Total\_Proposed}\right) = \sum_{k=0}^{N} \overline{m}_k t_{sim-k} \,, \tag{A.1}$$

where $\overline{m}_k$ is the average number of iterations a circuit is simulated at each given step and t_{sim-k} is the simulation time of the k^{th} verification step in the top-level verification phase. The two extreme steps correspond to the all behaviorally based macro-model and the all transistor-level simulations with 0 and N for k, respectively. The expected value for the simulation time of the conventional approach (i.e., a single, all transistor-based top-level simulation) is, on the other hand,

$$E\left(t_{Total\_Conv.}\right) = \overline{L}t_{sim-N} \,, \tag{A.2}$$

where $\overline{L}$ is the average number of iterations the top-level circuit is simulated and $t_{sim\text{-}N}$ is the simulation time of a single, all transistor-level run. The basic goal of the proposed strategy is for the expected value of the simulation time to be equal to or shorter than in the conventional approach, considering that iterations are necessary to identify problems and verify solutions. The premise here is that the number of iterations of the most time-consuming all-transistor circuit with the proposed strategy is low enough and its overall fault coverage large enough to merit its use,

$$\overline{m}_N < \overline{L}. \qquad \text{(A.3)}$$

Most errors, especially the ones due to connectivity, are typically found early in quick simulations since $t_{sim\text{-}0} < t_{sim\text{-}1} < ... < t_{sim\text{-}N}$, effectively decreasing the number of iterations required to simulate each subsequent step in the process (i.e., $\overline{m}_0 > \overline{m}_1 > ... > \overline{m}_N$), the net result of which is a reduction in the iterations required to simulate the costly all-transistor circuit (Figure A.4).

In practice, each sub-block in a system affects full transistor-level simulations differently and only a select few tend to be mostly responsible for prolonged computational times [141]. Therefore, verification time is minimized if less computationally intensive blocks are replaced earlier in the proposed process. Thus, the optimal replacement strategy is one where each subsequent mixed-signal simulation time $t_{sim\text{-}i}$ is the shortest possible out of all possible choices (Figure A.5).

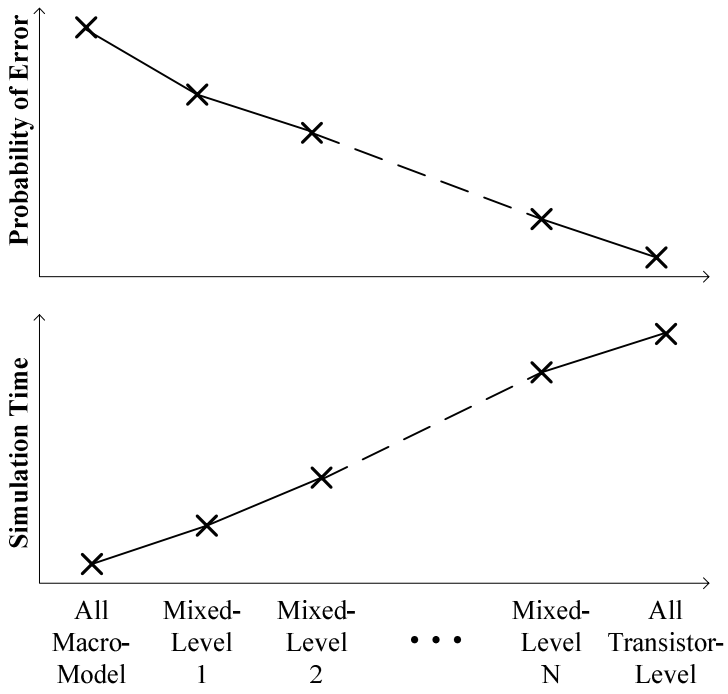


Figure A.4— Predicted simulation time and probability of finding errors at a given simulation step of the proposed strategy.

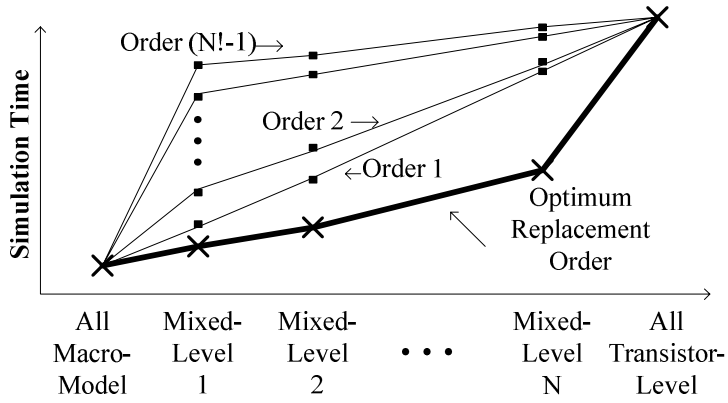


Figure A.5 — The proposed strategy verification time is minimized if circuit blocks are replaced based on their simulation time expense (i.e., optimum replacement order.

A.2.3. Determining the Optimal Replacement Order from a Set of Screening Simulations

The time it takes to finish a transient simulation is the summation of times each discrete step in the simulation incurs to compute a solution,

$$t_{sim} = \sum_{k=1}^{N_{Steps}} t_k \ , \qquad (A.4)$$

where N_{Steps} is the total number of steps in the simulation, which is controlled by the simulator to achieve a certain level of accuracy [145]. The computation time of each time step is mostly dominated by the time required to solve the matrix of equations for which the Newton-Raphson (NR) method is used until the solution satisfies the given time-step and NR tolerances,

$$t_k = (1 + N_{Time\text{-}Adj}) N_{Iteration} t_{NR} \ , \qquad (A.5)$$

where $N_{Iteration}$ is the number of iterations required to solve the NR matrix, t_{NR} is the time required to solve each matrix iteration, and $N_{Time\text{-}Adj}$ is the number of time-step adjustments used to satisfy $Step_{Tolerance}$ for each time step. Average simulation time $\overline{t_{sim}}$ is therefore

$$\overline{t_{sim}} = N_{Steps} t_{NR} \cdot \overline{(1 + N_{Time\text{-}Adj}) N_{Iteration}} \ , \qquad (A.6)$$

where $\overline{(1 + N_{Time\text{-}adj}) N_{Iteration}}$ is the average number of loop iterations at each step.

The t_{NR} is almost constant for a given topology and proportional to the number of circuit nodes cubed (i.e., nodes^3) [145], which explains why complex circuits have long simulation times. $N_{Iteration}$ depends on the linearity of the models, and the convergence of the NR method. N_{Steps} and $N_{Time\text{-}Adj}$ depend on frequency of operation of the circuits. As a result, a less complex circuit can be computationally more intensive if its transistor-level models superimpose a significant increase in N_{Steps}. Although predictions can be made about the effects of various blocks on simulation time, generally it is not possible to determine how the transistor-level model of each block slows down the simulation just by investigating netlist data (i.e., number of equations and nodes).

To determine the optimal replacement order, a screening set of simulations is proposed. The idea is to perform a set of mostly macro-level model simulations where only one macro model at a time is replaced with its respective transistor-level model (N simulations for N blocks). Consequently, the top-level blocks can be ranked and therefore replaced in the subsequent set of screening simulations according to their respective simulation times. Although screening simulations add overhead, they are only performed here to study the nature of the problem and project general conclusions, which are to be

drawn later. Consequently, these screening simulations are not part of the proposed verification process for ICs but simply the means through which an optimal replacement order is extracted for a general class of circuits.

A.3. Numerical Case Study Results

To evaluate the proposed strategy, a case study of a representative mixed-signal environment such as a current-mode, pulse-width modulated (PWM) buck (step-down) DC-DC converter (Figure A.1) is analyzed within the context of simulation time. The goal is to determine an optimal replacement sequence from a set of screening simulations. Evaluating the resulting replacement order will shed insight into the computational needs of the various components comprising the mixed-signal environment, especially switching regulators, most of which have similar functional units (i.e., error amplifier, comparators, bandgap reference, drivers and dead-time control, power train, and power-on-reset and related start-up control electronics).

The 0.5μm CMOS switching regulator circuit shown in Figure 1 was designed to convert a Lithium-Ion (Li-Ion) battery voltage (2.7 - 4.2 V) to a constant 1.5 V output voltage and source up to 1 A of load current at a switching frequency of 1MHz. The pertinent functional blocks of this design are the output power stage, signal generator, driver and dead-time control circuit, error amplifier, comparator, voltage reference, and power-on-reset block. The complete design process (i.e., system and block-level design and top-level verification) was executed within a Cadence platform, an industry standard. After the design was completely finished, simulations were repeated to ascertain and record simulation times and transient points of each mixed-level simulation step using Spectre simulator on an Ultra 10 Sun computer with *moderate* and *trapezoidal* tolerance and integration settings, respectively.

First, an all macro-model simulation of the system was performed, with the exception of the power stage for which no behavioral model was used, as discussed earlier in the text, because of its pivotal role and simplicity (e.g., consists of only a few electrical components). Then, screening simulations where only one macro-model at a time was replaced with its transistor-based equivalent in all macro-model simulation were performed (i.e., six simulations for six blocks), and their simulation time and

performance characteristics were recorded. The results of the screening simulations, which are tabulated in Table A.1, showed that the error amplifier incurred the least computational overhead on simulation time, followed by the comparator, bandgap reference, power-on-reset, driver, and wave generator circuits.

Next, the results of the screening simulations were verified against various mixed-level simulations. For instance, the screening results showed that the driver incurs more computation time than the power-on-reset block, and if this is indeed true, it follows that the driver incurs more time whether or not the error amplifier, comparator, and reference are replaced with their transistor-level models. Consequently, each of the remaining macro-models was replaced with their transistor-level equivalents, one at a time, and their simulation performance recorded and compared. This process was repeated for every subsequent step in the replacement sequence, resulting in a total of 22 simulations, one for all macro models, six for the screening process, five to verify the replacement order results of the next 5 circuit blocks (screening process for a subset of the blocks), four to very the results of the next 4 blocks, and so on, the outcome of which is also summarized in Table A.1. The results of all mixed-level simulations, from the five- to the two-block screening process, confirmed the consistency of the replacement order found with the first set of screening simulations, verifying the sequence to be in fact the optimal simulation arrangement.

Table A.1— Case study results of the top-level replacement sequence.

Blocks / Experiments	Power Stage	Amplifier	Comparator	Reference	Power-on-Reset	Driver	Signal Generator	No. of Nodes	No. of Equations	No. of BSIM Models	No. of Tran. Steps	Simulation Time (s)	Normalized Simulation Time
Start													
All Macro	T	M	M	M	M	M	M	138	221	24	186K	897	NA
Trial 1- *Screening Sim.*													
All Macro	T	M	M	M	M	M	M	138	221	24	186K	897	1x
Amplifier	T	T	M	M	M	M	M	136	200	86	186K	1.4K	1.6x
Comparator	T	M	T	M	M	M	M	154	214	94	186K	1.5K	1.72x
Reference	T	M	M	T	M	M	M	205	275	73	190K	1.8K	1.99x
Power-on-Reset	T	M	M	M	T	M	M	253	325	268	187K	3.6K	4.02x
Driver	T	M	M	M	M	T	M	173	242	128	122K	7.5K	8.32x
Signal Generator	T	M	M	M	M	M	T	313	287	391	190K	11K	13.2x
Trial 2													
All Macro - 1	T	T	M	M	M	M	M	136	200	86	186K	1.4K	1x
Comparator	T	T	T	M	M	M	M	148	196	122	186K	1.7K	1.22x
Reference	T	T	M	T	M	M	M	205	258	135	190K	1.8K	1.26x
Power-on-Reset	T	T	M	M	T	M	M	251	304	330	187K	4.1K	2.86x
Driver	T	T	M	M	M	T	M	167	224	156	120K	8.4K	5.83x
Signal Generator	T	T	M	M	M	M	T	313	370	453	190K	13K	9.08x
Trial 3													
All Macro - 2	T	T	T	M	M	M	M	148	196	122	186K	1.8K	1x
Reference	T	T	T	T	M	M	M	215	251	171	325K	3.3K	1.87x
Power-on-Reset	T	T	T	M	T	M	M	330	354	415	187K	7.8K	4.13x
Driver	T	T	T	M	M	T	M	179	220	192	134K	10K	5.70x
Signal Generator	T	T	T	M	M	M	T	323	362	489	189K	14K	7.85x
Trial 4													
All Macro - 3	T	T	T	T	M	M	M	215	251	171	325K	3.3K	1x
Power-on-Reset	T	T	T	T	T	M	M	330	354	415	327K	7.2K	2.18x
Driver	T	T	T	T	M	T	M	246	274	241	797K	9.6K	2.92x
Signal Generator	T	T	T	T	M	M	T	390	416	538	425K	13K	4.06x
Trial 5													
All Macro - 4	T	T	T	T	T	M	M	330	354	415	327K	7.2K	1x
Driver	T	T	T	T	T	T	M	361	378	485	802K	18K	2.53x
Signal Generator	T	T	T	T	T	M	T	505	525	782	428K	20K	2.67x
Last Step													
All Macro - 5	T	T	T	T	T	T	M	361	378	485	802K	18K	1x
All Transistor	T	T	T	T	T	T	T	536	544	852	650K	30K	1.66x

.

Figure 6 illustrates the transient response of the switching supply during its first 1.5ms of operation under a pulsing 0-1 A, 5 kHz, 50% duty-cycle load for the all macro- and all transistor-based top-level simulation. A single, all transistor-level simulation took more than eight hours to complete, when the all macro-model counterpart took less than 15 min. The macro models predict the DC (power efficiency and load and line regulation performance) and transient response of the switching regulator as accurately as the all transistor-level models. However, they do not verify other IC-related specifications like leakage, quiescent, and transient supply currents, all of which are sensitive to various parasitic in the system, like inter-block loading and short-circuit events, which is the inspiration behind the use of transistor-based models for the verification process in the first place. The results of the case study presented show that the transistor-level models of the signal generator and driver circuits account for approximately 60% of the total simulation time because of their high frequency spike and glitch content, and this is in spite of the relative simplicity of the driver block, which has less transistors, nodes, and working equations than the reference and power-on-reset functions. The transistor-level models of the analog building blocks (i.e., error amplifier, comparator, and reference) were only responsible for 11% of the total simulation time. Generally, linear analog blocks incur the least overhead, followed by nonlinear analog blocks like comparators and bi-stable bandgap references, low frequency digital functions like power-on-reset, and finally high speed driver and signal generator circuits. Within these broad categories, computation time of course increases with the number of working nodes, that is to say, with the number of transistors and therefore number of equations.

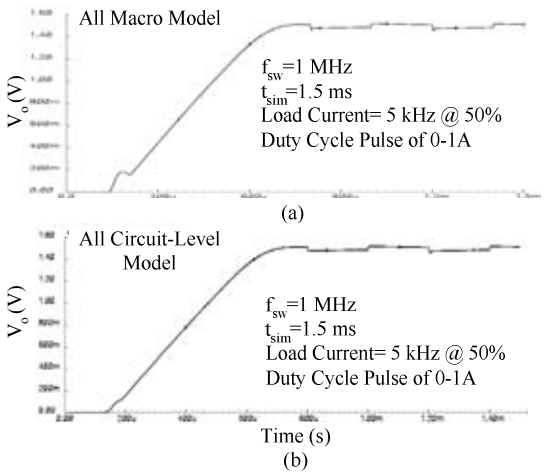


Figure A.6—Top-level transient waveforms of the (a) all macro- and (b) all transistor-based simulations.

According to the results of the case study, if the proposed strategy is used for top-level simulations, the screening simulation takes 460 minutes and following iterations of the mixed-level simulations incur 29, 54, 119, and 301 minutes, respectively, compared to the 499 minutes required by the all transistor-based simulation. Consequently, if no errors were to be found, the proposed sequence (mixed-level simulations and an all transistor-level simulation) incurs 1,017 min. of simulation time, which is equivalent to approximately two all-transistor-level simulations, yet at least 6 top-level simulations would be tested. And if a set of screening simulations were to be included, which is not a requirement, given the results of the study, the proposed sequence (screening simulation set, mixed-level simulations, and an all transistor-level simulation) incurs 1,462 min. of simulation time, roughly the equivalent of 3 all transistor-based top-level simulations, but actually verifying 11 simulations.

In practice, the benefits of the strategy are even more pronounced. Given, the complexity of the system, errors occur that invariably necessitate iterations, and iterations in the proposed scheme incur the least time (15 min. for the first level, 29 min. for the second, and so on). In fact, most top-level errors are the result of incorrect inter-block connections, which can be detected and corrected at the first level of the proposed sequence, when simulations take up about 15 min. As the replacement sequence advances, the design is cleared of these errors, leaving only a few all transistor-based top-

level simulations to perform to detect IC-related issues like leakage, quiescent, and transient supply currents. The proposed replacement sequence is therefore potentially capable of detecting many errors in the same time frame the traditional, all transistor-based simulation would have taken to detect less than a few. In the case of an extremely complex system, where all transistor-level top-level simulations are computationally prohibitive (e.g., simulation time of a few weeks because of convergence problems and such), the screening simulation suite can be used to capture top-level connectivity errors, in addition to determining the convergence culprit of the all-transistor top-level simulation. Isolating the convergence issue allows the designer to verify the rest of the system by simply replacing the problem circuit with its macro-model circuit.

The results of the case study generally apply to DC-DC converter circuits, given the similarity of the functional units. What is more, because of the qualitative nature of the blocks, the results can be further extrapolated to mixed-signal environments. More specifically, highly linear and analog blocks incur the least computational effort, whereas high frequency nonlinear blocks incur the most. Bandgap references are nonlinear analog blocks because they are bi-stable in nature (i.e., they require start-up circuits to ensure they work in the correct state) and are therefore more computational intensive than op-amps and even comparators. Start-up and low frequency digital blocks, which simply ascertain a state, require more simulation time than the reference but less time than high frequency digital circuits, which in turn require less time than more complex digital circuits (with feedback) like clock and ramp generators. Depending on how these characteristics apply to a given class of mixed-signal circuits, screening simulations may or may not be eliminated.

SUMMARY

Increasing fault coverage and decreasing simulation time of top-level simulations are conflicting requirements. To mitigate this adverse relationship, a series of mixed-level simulations have been proposed and verified, whereby each block of an all macro-model simulation is replaced with its equivalent transistor-level circuit, one at a time, with the least time-consuming blocks first. To determine the optimal replacement sequence, screening simulations were performed where an all macro-model setup was modified by replacing only one of its macro models with its respective transistor-level model, one at a

time. To verify this within the context of a mixed-signal environment, a switching buck regulator case was tested and evaluated, from which an optimal replacement order was determined. The results show the analog linear blocks are the least time-consuming, accounting for 11% of the total simulation time, and driver and signal generator circuits are the most time-consuming, accounting for approximately 60% of the time. These results can be extended to all DC-DC converter circuits because of the similarities of the functional blocks, and even some mixed-signal environments because of the nature of the effects – linear analog blocks incur less time than high frequency digital blocks with feedback. In the end, in the time that only three all transistor-based simulations are performed, more than 11 top-level simulations can be analyzed with the proposed strategy, which significantly increases the fault coverage in the same time. The benefits are even more pronounced when errors in the circuit exist, which the proposed strategy will more than likely catch earlier in the sequence and therefore incur less overall time to resolve.

APPENDIX B

PCB LAYOUT TECHNIQUES FOR SWITCHING POWER SUPPLY CIRCUITS

The demand for higher-performance switching regulators is relentless, requiring high power efficiency and accuracy, especially in battery-operated applications, such as laptops, cell phones, and personal digital assistants (PDAs). Efficiencies of more than 90% are required at both high and low loading conditions. Moreover, the output voltage ripple must be kept below tens of millivolts during all possible load transients. Significant effort has therefore been dedicated to devise techniques that improve power efficiency and accuracy of switching supply circuits [146, 147], and the incremental power efficiency improvement of any one of these techniques is normally less than 5%. However, these seemingly insignificant improvements are intrinsic and necessary to meet the stringent efficiency specifications of today's state-of-the-art applications.

The design of printed-circuit boards (PCBs) for high-current, fast-switching power converters requires more caution than ordinary PCBs, since the voltage drops caused by the parasitic impedances become significant in high current and fast-switching conditions. A PCB that is not well designed can degrade the power efficiency by up to 10% and increase the output ripple by tens of millivolts, thereby reducing accuracy performance. To compensate for a poorly designed PCB, design and application engineers must develop additional circuitry and/or upgrade their external components (e.g., low-resistance power switches, low ESR inductors, low ESR ceramic capacitors, etc.), which not only increases design time but also overall system cost.

There are many well-known references on the design and analysis of switching power supplies, but little [148-150] to no discussion [151-153] is offered on the design aspects of the printed-circuit boards (PCBs). Most of the literature on the design of PCBs for switching supplies is found in a few obscure application notes [154-161], and most of the guidelines are oriented specifically to a commercial product, outlining an application-specific layout plan, not general design guidelines.

The objective of this paper is to provide a tutorial and instructional material on PCB design of fast-switching, high-current power supplies for students, technicians, researchers, and engineers who are not experts in the field of power supplies. A sample switching power supply circuit is used to highlight and extrapolate the various design considerations of PCBs for high power circuits. The guidelines are derived from the circuit directly such that the techniques used to address them can be extended to other circuits under similar design constraints, in other words, high power circuits.

B.1. Modeling Connections

In practice, electrical nodes are not dimensionless, zero-impedance junctions. They are metal links with resistive, inductive, and capacitive properties that vary significantly with PCB layout. An area of metal used to connect two electrical points can be modeled with a simple impedance network consisting of a resitor, inductor, and capacitor combination, as shown in Figure B.1. The parasitic capacitance to ground is normally negligable, when compared to the capacitors typically used in power supply circuits (e.g., 1 nF to 100 µF). An area of metal used to link three ports is similarly modeled with the triangular impedance network shown in Figure B.2(a), where each impedance consists of a parasitic inductor in series with a parasitic resistor, neglecting the parasitic capacitors because of the aforementioned reason. Increasing the width of the links, as done in Figure B.2(b), do not alter the circuit model, even when the width is large enough to eliminate the separation between the links (Figure B.2(c)). The corresponding impedance values are the only ones that change. Generally, the connection can have any arbitrary shape, including an irregular chunk of solder, as illustrated in Figure B.2(d).

The triangular model can always be mapped into an equivalent star network, and vice versa (Figure B.3). The dimensionless, zero-impedance node in the middle of the star network is only conceptual and is not literally accessible on the PCB. An “n” port connection can be decomposed into two- and three-port sections, and a star model can be used for each of these segments, as shown in Figure B.4.

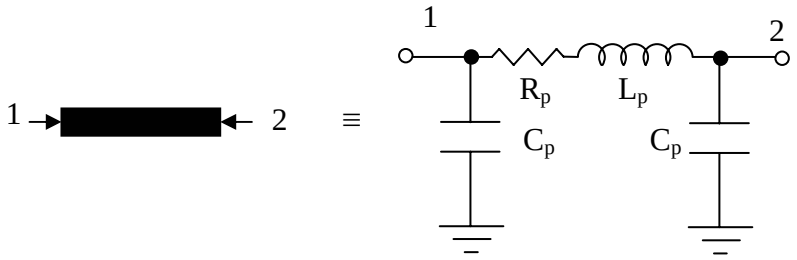


Figure B.1—Electrical modeling of a two-port connection.

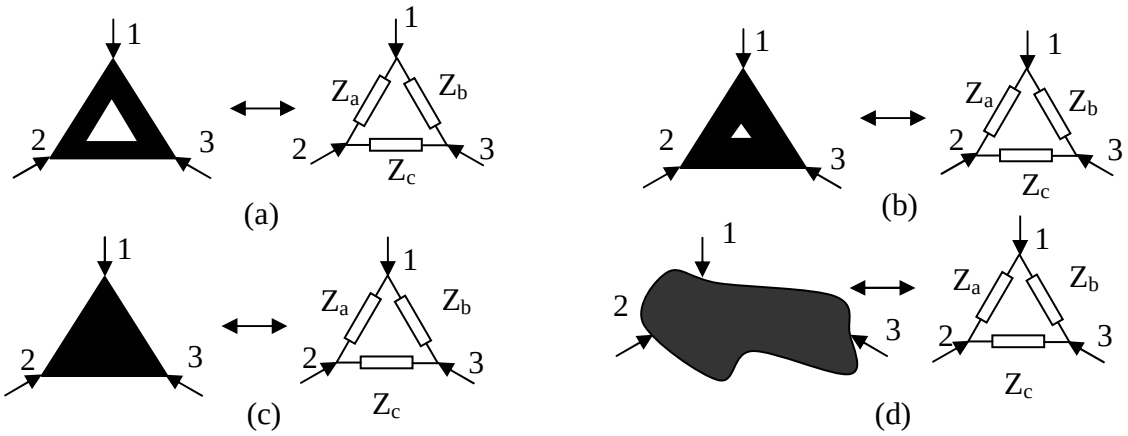
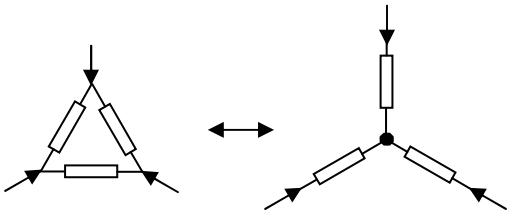


Figure B.2— Modeling high-current fast-switching connections: (a) model for a triangular three-port surface with a large opening in the middle, (b) model for a triangular three-port surface with a small opening, (c) model for a solid triangle, and (d) model for an arbitrary slab of solder.

$$Z_{12} = Z_1 + Z_2$$
$$Z_{13} = Z_1 + Z_3$$
$$Z_{23} = Z_2 + Z_3$$



$$Z_1 = \frac{Z_a Z_b}{Z_a + Z_b + Z_c}$$
$$Z_2 = \frac{Z_a Z_c}{Z_a + Z_b + Z_c}$$
$$Z_3 = \frac{Z_b Z_c}{Z_a + Z_b + Z_c}$$

Figure B.3—Triangle-to-star impedance network conversion.

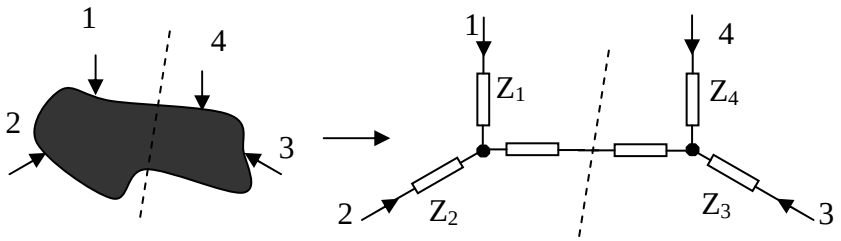


Figure B.4— An impedance model for a four-port connection.

To extract the pertinent star model parameters, the impedance between any two points is measured, while leaving the remaining terminals disconnected. Through inspection, the measured impedance between any two points in the triangular model (e.g., Z_{12}) is the parallel combination of the direct impedance between the two points (e.g., Z_a) and the series impedance combination going through the third point in the triangle (e.g., $Z_b + Z_c$), which is how the triangle model maps into a star network:

$$Z_{12} = Z_a \parallel (Z_b + Z_c) = \frac{Z_a Z_b + Z_a Z_b}{Z_a + Z_b + Z_c} = Z_1 + Z_2 \,. \qquad \text{(B.1)}$$

Measuring the impedance between terminals one and two, two and three, and one and three yield $Z_1 + Z_2$, $Z_2 + Z_3$, and $Z_1 + Z_3$, respectively, which are readily solved (three equations and three unknowns).

The actual resistance and inductance of a PCB metal trace with length l, width w, and height h in meters are

$$R = \rho\left(\frac{l}{wh}\right) \qquad \text{(B.2)}$$

and

$$L = 2l\left[\ln\left(\frac{2l}{w+h}\right) + 0.5\right]10^{-7}\,H\,, \qquad \text{(B.3)}$$

where ρ is the metal line resistivity (1.724e-8Ω·m for copper) [162]. The inductance is an approximation because components in its proximity will also affect its value. As a rule of thumb, every 2.5cm (one inch) of 0.25mm (10mil) wide and 0.035mm (1.4mil) thick copper trace has 20mΩ of resistance and about 20nH of inductance [154]. Consequently, both a 1A per 1μs change in current and a 1A DC will independently cause a 20mV drop across the aforementioned trace ($V = Ldi/dt + I_{DC}R$). High current, fast-switching signals are therefore critical, not only do they incur the resistive but also the transient inductive

voltage drop, which could be worse (e.g., 1A/10ns through a 20nH inductor incurs a 2V drop). The inductive voltage drop fades away after the transition is over, but its mere occurrence can still disturb the functionality of the system and damage various parts of the power supply, especially the sensitive ICs because of various failure mechanisms, such as minority carrier injection or latch up [163]. To reduce these ill-fated effects, in other words, decrease the parasitic resistance and inductance of the trace, the trace should be short and wide (Equations B.2 and B.3). However, an increase in width is not as effective as a decrease in length because of the logarithmic term.

As an example, to illustrate how to model and ascertain the parasitic effects of any given connection on a PCB, the ideal buck-switching regulator illustrated in Figure B. 5(a) is used, but the process and procedure used here is naturally extended to any high power PCB application. The circuit consists of various power and control components, consisting of power MOSFET M_p, power diode D_p, output capacitor C, power inductor L, input capacitor C_{in}, and a controller IC. The battery and loading application are connected to the input and output of the regulator, respectively. Figure B.5(b) illustrates how every connection in the converter shown in Figure B.5(a) is modeled with a star network, where each impedance is a parasitic resistor-inductor combination. The electrical components of the circuit also have parasitic effects, most important of which are normally their equivalent series resistors (ESRs) (e.g., inductor and capacitor ESR).

Figure B.5(a) also illustrates the high-current and fast-switching paths, which are of particular interest, given their significant parasitic effects. The MOSFET and diode currents, for instance, are pulsating in nature, as also shown in the figure, switching from zero to the inductor current level in a few nanoseconds. These currents are therefore both high current and fast switching, which is why reducing their pertinent parasitic resistance and inductance values is extremely important. The output capacitor, on the other hand, only carries the inductor current ripple, which is neither relatively high in value nor fast, and higher parasitic inductance is therefore tolerated in the metal link between the inductor and the output capacitor.

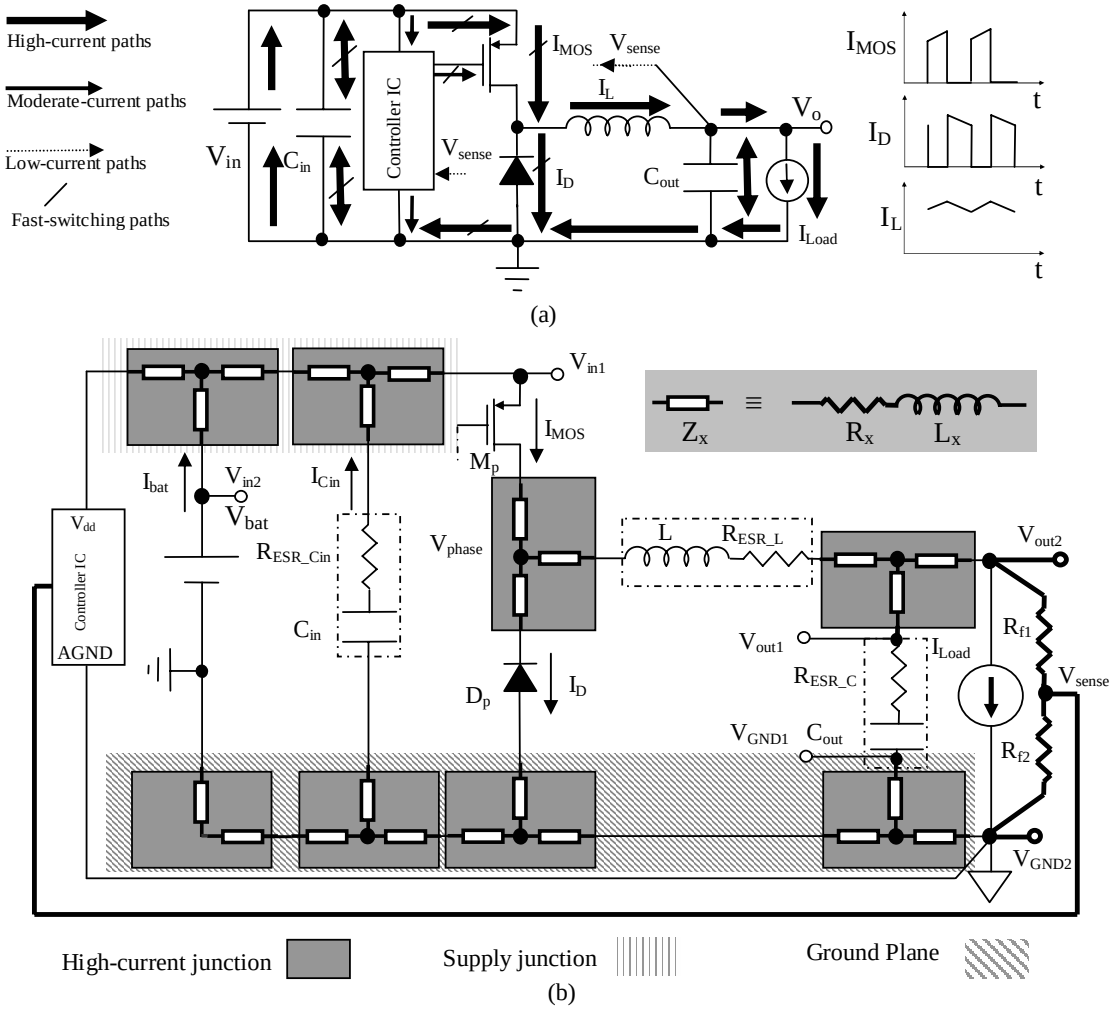


Figure B.5— (a) High-current and fast-switching paths and (b) parasitic resistors in a buck DC-DC converter circuit.

These parasitic impedances can severely affect the performance of a system, from a malfunction to degraded power efficiency and reduced accuracy. The large voltage spikes across the parasitic inductors can potentially reverse-bias and damage internal silicon p-n junctions present in the control circuitry. What is more, the power losses associated with the parasitic resistors has a direct bearing in overall power efficiency, which is especially critical in portable electronics for extended battery life. The parasitic PCB resistance series with the output capacitor's ESR not only has this effect but also

degraded accuracy and altered filtering characteristics, which of course affects feedback stability.

B.2. PCB Layout Guidelines

Layout techniques for switching power supplies are divided in two general categories: those that affect circuit performance and those related to electro-magnetic compliance (EMC). The former addresses the functionality, accuracy, and efficiency of the circuit and the latter is mostly targeted to ensure the circuit passes EMC tests. While the guidelines assume the power switches and diode are off-chip, the same rules apply to controller ICs with on-chip power components. What is more, these guidelines, at a smaller scale, also apply to the IC itself, to the "PCB" within the chip.

B.2.1. Functionality

Parasitic resistors in high-current paths and parasitic inductances in fast switching signal traces can potentially upset the circuit operation of the system. Consequently, for the sample buck-supply circuit shown in Figure B.5, the most important connection is the phase junction that connects the power inductor to the switches (V_{phase}), since it carries fast-switching currents in the order of amperes. The trace connecting the input capacitor, the input supply's positive terminal, and the power MOSFET's source as well as the connections from the diode to power ground carry high current and fast switching signals (Figure B.5). As explained in Section B.1, short and wide routing traces have lower parasitic resistances and inductances and therefore superimpose less ill-fated effects to the system. As a result, to reduce parasitic resistance and inductance, the first rule in PCB layout is to place connected power components (i.e., C_{in}, M_p, D_p, L, and C_{out}) as close as possible, and in a way that their interconnection lengths are minimal [153]. The width of all high-current paths should be sufficiently wide to exhibit low resistive values, when compared to the power components. For example, if the power switch's resistance is 70 mΩ, the PCB's trace resistance should be less than 10 mΩ so as not to incur significant additional power losses. Moderate current-carrying paths, like the path from the MOSFET's gate driver to the MOSFET's gate, also warrant some attention because of their peak switching current characteristics. The issues that apply to high current, fast-switching paths also apply to moderate current-carrying paths, but in a less critical

fashion; in other words, they have lower priority. The width of PCB lines can therefore be somewhat smaller and their length longer, implying slightly higher resistance and inductance values and therefore giving the designer more flexibility to address fast-switching, high-current paths first.

Additional precautions should be employed in the design of evaluation boards (e.g., EVM). In these boards, which are many times used to test and gauge switching supply circuits, the power supply and the system load are not on the PCB. They are connected to the board via lead wires and connectors, which introduce series resistors and inductors. In a portable application, the power supply (e.g., battery) and the load may be on the same PCB, and no additional lead wires may be needed. In such cases, the parasitic components of the leads are not present.

Another important issue is to use separate, parallel connections for the supply ground, load ground, and measurement instrument's ground, instead of series connections. Series connections are unreliable and lossy, and they introduce additional undesired impedance between critical nodes. Undesired noise and high temperature gradients across the PCB usually result when problems with supply ground connections exist.

B.2.2. Accuracy

Power supply circuits regulate the supply voltages of loading applications against variable input supply variations and across operating conditions, making accuracy a key performance parameter. For maximum accuracy, the feedback sense terminal should be connected as close to the load as possible, since the voltage across the load is the one requiring regulation (Figure B.5). Although this connection of the feedback network ensures output DC accuracy, the output ripple during steady-state conditions and load transient events are functions of PCB parasitic impedances, as will be shown. During normal operation, the inductor current is the summation of load current I_{DC1} and capacitor ripple current I_c (Figure B.6(a)). Since the rate of current change in steady state is relatively small (e.g., in the order of 1 A per µsec), the voltage drops across the parasitic inductors are negligible. Moreover, the voltage drops across load connections ($R_{PCB\text{-}ld+}$

and $R_{PCB\text{-}ld\text{-}}$) are constant since the load current is constant in steady-state. Consequently, the voltage ripple across the load is

$$V_{out\text{-}AC}(t) = I_c(t)(R_{PCB\_C+} + R_{PCB\_C-} + R_{ESR\_C}) + \frac{1}{C_{out}}\int I_c(t)dt\,, \qquad \text{(B.4)}$$

where R_{ESR_C} is the output capacitor's ESR and R_{PCB_C+} and R_{PCB_C-} are the PCB parasitic resistors used to connect the capacitor to the circuit. Ripple current $I_c(t)$ is a function of input voltage V_{in}, output voltage V_o, inductor L, and the switching frequency of the supply circuit, and is independent of the output capacitor and load, since the output voltage is for all practical purposes constant in steady state. The ripple voltage across the output capacitor is usually small because of its high capacitance. The output voltage ripple is therefore mostly composed of the capacitor's ESR and the parasitic PCB resistances.

In constant frequency controllers such as pulse-width modulated (PWM) controllers [147-150], the inductor ripple current is fixed because the switching frequency is constant. As a result, inductor ripple current (I_c) is constant and the steady state output ripple voltage is increased if parasitic resistors are increased (Eq. (B.4)). However, in constant ripple voltage controllers like hysteretic converters [147], the change in parasitic resistances manifests itself in a variation of switching frequency, which results in lower overall efficiency (e.g., an increase in equivalent capacitor ESR from 10mΩ to 20mΩ doubles the switching frequency and switching losses). Hence, to increase both ac accuracy and power efficiency, both in the case of PWM and hysteretic power supply circuits, the PCB should be designed such that R_{PCB_C-} and R_{PCB_C+} are minimal.

The effect of PCB parasitic impedances becomes even more important during load transients. If the load current changes abruptly, from I_{DC1} to I_{DC2} in nano seconds, the inductor current and supply circuit cannot respond fast enough to fully comprehend the change. Thus, the output capacitor (C_{out}) supplies all the transient current, simplifying the output stage to just a passive LCR filter (Figure B.4(b)). The maximum instantaneous output voltage ripple happens at the end of a load-current change, when load current has just reached I_{DC2}. Since the output capacitor is large, its output voltage does not change significantly, and hence the transient ripple voltage mostly consists of the resistive

voltage drops across the parasitic resistors (V_{INST-R}) and the inductive voltage spikes across the parasitic inductors (V_{INST-L}), which results in

$$V_{INST} = V_{INST\_L} + V_{INST\_R} =$$

$$(L_{PCB\_C+} + L_{PCB\_C-} + L_{PCB\_ld+} + L_{PCB\_ld-}) \frac{I_{DC2} - I_{DC1}}{t_r} \qquad \text{(B.5)}$$

$$+ (R_{PCB\_C+} + R_{PCB\_C-} + R_{PCB\_ld+} + R_{PCB\_ld-})(I_{DC2} - I_{DC1}) .$$

After the transient condition, the inductive drop is shunted by an LCR tank (i.e., parasitic L, parasitic R, and C_{out}), and the output voltage drop retains its V_{INST-R} value (Figure B.6(b)). After the initial drop sequence, the output voltage continues to drop slowly because the output capacitor slews (i.e., discharges). After a delay time proportional to the inverse of controller bandwidth, the controller kicks in and starts to recharge the capacitor to reach the desired steady state operation. Although the drop due to the capacitor discharge can be limited by designing output capacitor value and the controller loop bandwidth, the instantaneous voltage drop (V_{INST}) is independent of DC-DC converter control circuitry and is strongly PCB design dependent. From Equation 4, the worst-case instantaneous ripple occurs when the output current changes abruptly from zero to full load or vice versa. To minimize the instantaneous drop, the output capacitor should be placed as close as possible to the load, and therefore for a specified transient accuracy, the designer should pay special attention in routing the trace that connects load to output capacitor.

B.2.3. Noise

Switching nodes and traces of a DC-DC converter can inject noise to the analog and sensitive traces through capacitive coupling. The traces that are connected to high-impedance nodes are more sensitive to pickup environmental noise. To increase noise immunity, the traces connected to high impedance nodes should be routed as short as possible and placed as far as possible from noisy traces. For example in Figure B.5(b), V_{sense} voltage at the resistor dividers is connected to the high impedance input of error amplifier in the controller. Therefore, resistors R_{f1} and R_{f2} should be placed close to the chip and far from noisy phase node (V_{phase}) to increase noise immunity of sense voltage.

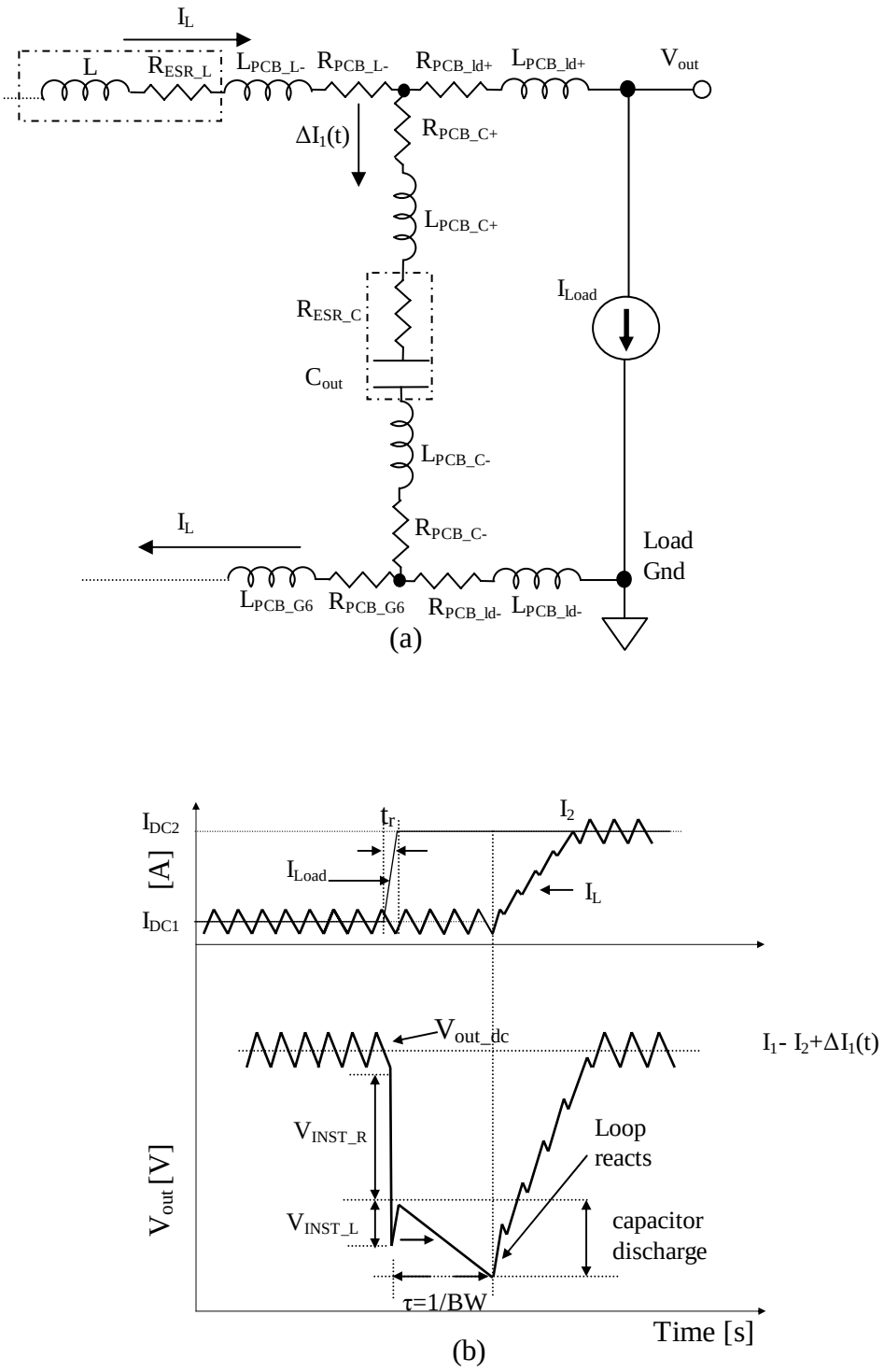


Figure B.6— (a) Equivalent circuit and (b) output voltage waveform during a current load transient for a buck converter

B.2.4. Radiated Electro-Magnetic Interference (EMI)

Radiated electro-magnetic interference (EMI) is another important issue to consider in the layout design of power circuits. Due to industry standards, the amount of

electro-magnetic power propagated from a commercial circuit through radiation should be limited. This limitation minimizes the interference among electric systems when they are working in close proximity [164, 165]. Nodes with fast switching voltages and/or currents generate radio-frequency (RF) noise (e.g., the V_{phase} node in a buck converter has nano-second rise and fall times). In general, any trace containing an ac current generates time-varying magnetic fields around it, producing time-varying electric fields and consequently radiating EMI.

To limit the electro-magnetic radiation from the PCB, two important guidelines should be considered. First, high frequency switching nodes should be as short as possible. The metal paths act as antennas and their frequency range is directly proportional to their length (i.e., shorter paths cover lower frequency ranges). Second, high frequency signal-return paths should be as close as possible to their respective forward paths. The two traces will therefore generate equal but opposite magnetic fields, canceling each other and hence reducing radiated EMI.

Although a strong recommendation for using ground planes exists (i.e., filling every available space on the PCB with copper and connecting to ground), the use of a ground plane may not be effective in all instances [154]. Ground planes are effectively close high-speed return paths for average forward signal paths, but arbitrarily increasing the ground plane may not necessarily reach critical nodes. In PCB technologies with more than two layers, middle layers are normally dedicated to ground planes, thereby decreasing their distance to high-current forward switching paths. Large metal areas connected to the controller pins also help conduct thermal energy from the chip to the surrounding air, resulting in lower junction-to-ambient thermal impedance and consequently reducing power losses, decreasing operating temperatures, and increasing reliability. This is especially important with controller chips that use on-chip power switches [158, 159]. In a buck converter, for instance, careful attention should be paid to the switching phase node and other fast-switching traces carrying high MOSFET and diode currents to minimize EMI propagation.

The trace connecting a driver circuit to the gate of a power MOSFET switch also requires scrutiny [151, 164-165]. During the power MOSFET's off to on transition, the driver circuitry charges the gate of power MOSFET with more current than is usually

necessary, which results in damped oscillations in the presence of a parasitic inductance in the gate trace. The damping frequency is usually an order of magnitude higher than the on/off transitional frequency ($1/t_{rise}$ and $1/t_{fall}$ where t_{rise} and t_{fall} are rise and fall times of the switch's controlling node, the gate in the case of MOSFETs). Since the power MOSFET is a large device, relatively high energy is involved in the on/off events, radiating EMI and possibly causing the power supply to fail EMC tests at high frequencies. To eliminate this effect, a series resistor can be placed in series with the power MOSFET's gate to limit the current during the on/off transitions.

B.3. Measurements

B.3.1. Test Points

Caution must be exercised when connecting measurement instruments' leads to the PCB. In Figure B.5(b), the proper measurement points to test a DC-DC converter circuit, not to a PCB, are labeled as V_{in1}, V_{out1}, and V_{GND1}. To measure the output voltage, the oscilloscope ground should be connected to the ground plane, as close as possible to the capacitor, feedback, and load ground. Similarly, the oscilloscope probe should be connected to the output node as close as possible to the filter capacitor, feedback resistor, and load nodes. To measure the input voltage level, the input node voltage in the PCB closest to the MOSFET source is preferred. The aforementioned technique eliminates the effect of lead parasitic resistances in computing the efficiency. If the PCB is included in the test, the oscilloscope lead should be connected to the supply, ground, and output planes, which are illustrated by V_{in2}, V_{out2}, and V_{GND2} in Figure B.5(b).

B.3.2. Ground Loops

A potential measurement problem in the process of power supply measurements is the ground loop situation [153]. A ground loop occurs when there is more than one ground path from the supply ground to the load ground. Test and measurement equipments have a safety connection to "earth" ground by the bench, which may cause undesirable connections between various ground points in the circuit. The oscilloscope ground is usually connected to the workbench earth. The supply voltage ground and the load ground may or may not be connected to the earth ground. The effect of a ground

loop in the behavior of the system is graphically illustrated in Figure B.7. The oscilloscope and power supply are not isolated from the workbench "earth" in this scheme. The oscilloscope measures the voltage difference at its inputs (V_{ch1} and V_{GND}), but the oscilloscope probe is connected to V_{LGND} and V_o at converter. Because of probe high impedance at V_{ch1}, there is no significant voltage drop between V_{ch1} and V_o. Nevertheless, the load current (I_{Load}) can return to the battery negative terminal through both the designed ground plane or from the workbench earth through probe ground wire. As a result, current flowing through probe parasitic resistance and inductance (R_{probe} and L_{probe}) generates a voltage drop between V_{GND} and V_{LGND}, which distorts the measured waveform. Therefore, circuit performance is underrated.

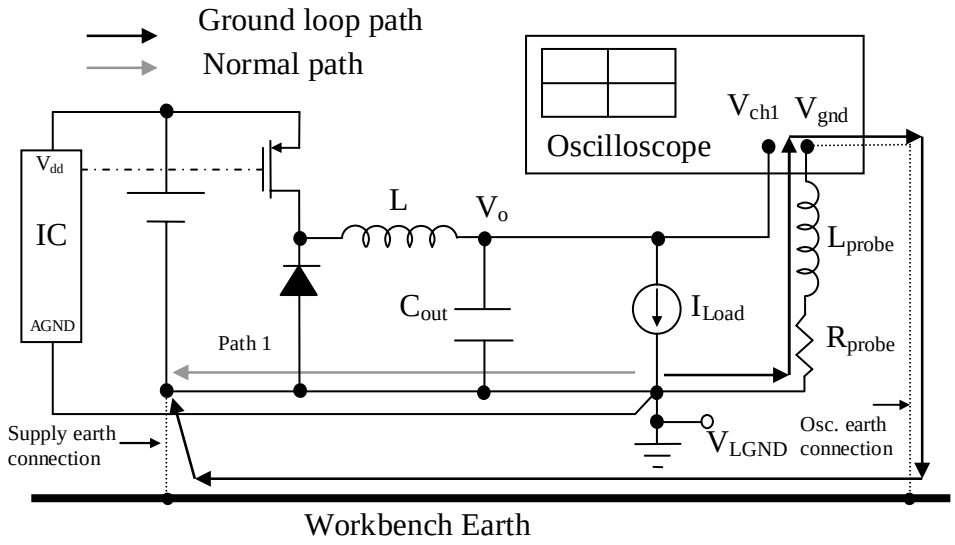


Figure B.7— Illustration of ground loop problem: if the oscilloscope and power supply are not isolated, the oscilloscope probe ground conducts high switching current and generates an unwanted voltage drop across the ground probe lead and the oscilloscope ground.

There is a simple way to test if a ground loop problem exists in the measurement system. While the DC-DC converter is operational, if the oscilloscope probe lead and its ground are connected to the ground plane and the noisy spikes at the switching frequency of the converter are seen on the oscilloscope display, the ground connection is not good, and a ground loop problem exists. To prevent this ground loop problem, the oscilloscope should be isolated from the bench. Either an isolation transformer can be applied to supply the oscilloscope or a differential probe can be used to isolate the probe ground from "earth." Another approach is to use floating supplies and loads.

SUMMARY

This chapter presented a guideline for PCB layout design of high-performance power supply circuits. Instead of describing a set of rules that are applicable only to a special circuit topology, the material provides general PCB layout design guidelines and how they address the various important performance parameters of high-current, fast-switching applications, using a switching power supply circuit as an example. The approach is first to model the parasitic trace impedance of connections and then study their effects on the functionality and key performance specifications, such as accuracy, efficiency, and electro magnetic compliance (EMC). After analyzing and prioritizing the various error sources, PCB layout guidelines for placing components and routing traces were derived, as summarized in Table B.1.

Table B.1—Summary of circuit-driven PCB design approach.

	Culprit	Approach
Functionality	**Parasitic L** **Parasitic R**	▪ Reduce parasitic inductances in fast-switching current paths to suppress unwanted $L_{par}di/dt$ voltage drops. ▪ Reduce parasitic resistances in high-current paths to eliminate unwanted $R_{par}I$ voltage drops. ▪ Priority is with fast-switching connections since $L_{par}di/dt$ dominates if switching frequency is high. ▪ Place power components as close as possible to each other. ▪ Reduce the parasitic inductances and resistances by routing them as short and wide as possible.
Efficiency	**Parasitic R**	▪ Reduce parasitic resistances in high-current paths. ▪ Place power components as close as possible to each other to reduce the length of connections. Route their connections as wide as possible.
DC Accuracy	**Parasitic R**	▪ Connect the Controller IC output voltage sense and analog ground pins as close as possible to the load. ▪ Place the output capacitor as close as possible to the load to suppress the parasitic resistances between load and output capacitor. As a result, the ac ripple is reduced.
Transient Accuracy	**Parasitic R** **Parasitic L**	▪ Reduce the parasitic resistance and inductance between output capacitor and the load to reduce voltage drops across parasitic inductors and resistors at load transients.
Switching Noise Injection	**Parasitic C**	▪ Route sensitive connections connected to high impedance nodes as short as possible. ▪ Route them as far as possible from noisy signals to reduce capacitor coupling to noisy signals. ▪ The trace that connects the sensed output voltage from feedback resistors to the input of controller error amplifier is “the” sensitive connection in switching regulators.
EMI		▪ Route fast-switching connections as short as possible. ▪ Route return paths of fast switching connections close to their forward paths. ▪ Priority is with routing connections that their currents change suddenly (fast-switching currents). ▪ Fill empty spaces with ground plane.
Test & Measurement		▪ Beware of ground plane changes because of connecting test and measurement instruments to the converter circuitry. Avoid ground loops by: - Floating supplies and loads - An isolated oscilloscope

REFERENCES

Chapter 1

[1] D. Arnold, *Magnetic Machines for Micro Engine Power Generation.* PhD Thesis, Atlanta, GA: Georgia Institute of Technology, 2004.

[2] M. Chen and G. Rincón-Mora, "A self-powered, self-sustaining system-on-chip (SOC) solution powered from hybrid micro-fuel cells," *Proc. 2004 Army Science Conference*.

[3] A. Lal and J. Blanchard, "Daintiest dynamos," *IEEE Spectrum*, Sept. 2004, pp. 36-41.

[4] E. Torres and G. Rincón-Mora, "Long lasting, self-sustaining, and energy-harvesting system-in-package (SiP) sensor solution," *Proc. 2005 International Conference on Energy, Environment, and Disasters (INCEED).*

[5] H. Pishronik, *Applications of Random Graphs to Design and Analysis of LDPC Codes and Sensor Networks.* PhD Thesis, Atlanta, GA: Georgia Institute of Technology, 2005.

[6] B. Sahu and G. Rincón-Mora, "A high efficiency, linear RF power amplifier with a power-tracking, dynamically adaptive buck-boost supply," *IEEE Transactions on Microwave Theory and Techniques,* Jan. 2004.

[7] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, NY: Wiley, 2001.

[8] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[9] G. Rincon-mora, "DC-DC converters: a topology journey," tutorial presented at *45th Midwest Symposium on Circuits and Systems (MWSCAS)*, Tulsa, OK, Aug. 2002.

[10] H.P. Forghani-zadeh and G.A. Rincón-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. 2002 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 577-580.

[11] R. Lenk, **"**Application bulletin AB-20 optimum current-sensing techniques in CPU converters," *Fairchild Semiconductor Application Notes*, 1999.

[12] W. Schults, "Lossless current sensing with SENSEFET enhance the motor drive," Motorola Technical Report, 1988.

[13] S. Yuvarajan, "Performance analysis and signal processing in a current sensing current MOSFET (SENSEFET)," in *Proc. 1990 Industry Applications Society Annual Meeting*, pp. 1445–1450.

[14] P. Givelin, M. Bafleur, "On-chip over-current and open-load detection for a power MOS high-side switch: a CMOS current-source approach," in *Proc. 1993 European Conference on Power Electronics and Applications*, pp. 197 –200.

[15] S. Yuvarajan and L. Wang, "Power conversion and control using a current-sensing MOSFET," *in Proc. 1992 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp.166 –169.

[16] J. Chen, J. Su, H. Lin, C. Chang, Y. Lee, T. Chen, H. Wang, K. Chang, and P. Lin, "Integrated current sensing circuits suitable for step-down DC-DC converters," *Electronics Letters*, vol. 40, Feb. 2004, pp. 200-201.

[17] C. Lee and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid States Circuits*, vol. 39, Jan. 2004, pp. 3-14.

[18] E. Dallago, M. Passoni, and G. Sassone, "Lossless current-sensing in low-voltage high-current DC-DC modular supplies," *IEEE Transactions on Industrial Electronics*, vol. 47, Dec. 2000, pp. 1249-1252.

[19] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE Journal of Solid States Circuits*, vol. 38, Mar. 2003, pp. 450-459.

[20] "Databeans says TI is still the top analog supplier," *Planet Analog*, [online document], Jun. 2005, [cited 2006 Apr. 1], Available HTTP: http://www.planetanalog.com/showArticle.jhtml?articleID=60407539

[21] Nathan Andrews, “Power: Rising from '01's ashes,” *Planet Analog*, [online document], Jul. 2005, [cited 2006 Apr. 1], Available HTTP: http://www.planetanalog.com/showArticle.jhtml?articleID=18307328

[22] “iSuppli: Power management market okay for now, but expect things to get ugly,” *Power Management Design Line,* [online document], Apr. 2005, [cited 2006 Apr. 1], Available HTTP: http://www.powermanagementdesignline.com/news/161501046

[23] “Tech Focus: Analog ICs,” *Power Management Design Line,* [online Document], Jul. 2000, [cited 2006 Apr. 1], Available HTTP: http://www.my-esm.com/showArticle.jhtml?articsleID=2908870

[24] “iSuppli Webinar: Power Management Outlook for 2005,” *Power Management Design Line,* [online document], Feb. 2005, [cited 2006 Apr. 1], Available HTTP: http://www.powermanagementdesignline.com/showArticle.jhtml?articleID=60401446

[25] “China’s Analog Market Races Ahead,” *Databeans*, [online document], Jul. 2005, [cited 2006 Apr. 1], Available HTTP: http://www.databeans.net/Newsletters/newsletter-Current.htm

[26] C. Pynn, “Analyzing manufacturing test costs,” *IEEE Design & Test of Computers*, Jul. 1997, pp 36-40.

[27] R. Schuke and K. Pande, “Manufacturing cost analysis of optoelectronic integrated circuits,” *IEEE Transactions on Test and Manufacturing*, Feb. 1989, pp. 29-31.

[28] D. Becker and P. Sandborn, “On the use of yielded cost in modeling electronic assembly processes,” *IEEE Transactions on Electronics Packaging and Manufacturing*, Jul. 2001, pp. 195-202.

[29] Intel, *VRM 9.1 DC-DC converter design guidelines.* Santa Clara, CA: Intel Corporation, Jan. 2002.

[30] E. Torres, L. Milner, N. Keskar, M. Chen, H. Pan, V. Gupta, P. Forghani, and G.A. Rincón-Mora, “SiP Integration of Intelligent, Adaptive, Self-Sustaining Power Management Solutions for Portable Applications,” *in Proc. IEEE 2006 International Symposium on Circuits and Systems (ISCAS).*

[31] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[32] G. Rincon-Mora, "DC-DC converters: a topology journey," *tutorial presented at 45th Midwest Symposium on Circuits and Systems (MWSCAS)*, Tulsa, OK, Aug. 2002.

[33] Current-sharing techniques for VRMs, *Technical Brief TB385.1*, Milpitas, CA: Intersil Corporation, 2001.

[34] M. Gildersleeve, H.P. Forghani-zadeh, and G. Rincon-Mora, "A comprehensive power analysis and a highly efficient, mode-hopping DC-DC converter," in *Proc. 2002 Asian-Pacific Conference on ASICs*, pp. 153-156, 2002.

[35] L.A. Milner and G.A. Rincón-Mora, "A novel predictive inductor multiplier for integrated circuit DC-DC converters in portable applications," in *Proc. 2005 International Symposium on Low Power Electronics and Design (ISLPED).*

[36] W. Ki and D. Ma, "Single-inductor multiple-output switching converters," *in Proc. 2001 IEEE Power Electronics Specialists Conference (PESC),* pp. 226-231.

[37] R. Lenk, **"**Application bulletin AB-20: optimum current-sensing techniques in CPU converters," *Fairchild Semiconductor Application Notes*, 1999.

[38] W. Schults, "Lossless current sensing with SENSEFET enhances the motor drive," *Motorola Technical Report*, 1988.

[39] S. Yuvarajan, "Performance analysis and signal processing in a current sensing current MOSFET (SENSEFET)," in *Proc. 1990 Industry Applications Society Annual Meeting*, pp. 1445-1450.

[40] P. Givelin, M. Bafleur, "On-chip over-current and open-load detection for a power MOS high-side switch: a CMOS current-source approach," in *Proc. 1993 European Conference on Power Electronics and Applications*, pp. 197-200.

[41] S. Yuvarajan and L. Wang, "Power conversion and control using a current-sensing MOSFET," *in Proc. 1992 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp.166-169.

[42] J. Chen, J. Su, H. Lin, C. Chang, Y. Lee, T. Chen, H. Wang, K. Chang, and P. Lin, "Integrated current sensing circuits suitable for step-down DC-DC converters," *Electronics Letters*, Feb. 2004, pp. 200-201.

[43] C. Lee and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid State Circuits*, vol. 39, Jan. 2004, pp. 3-14.

[44] C. Xiao, L. Zhao, T. Asda, W. Odendaal, and J. van Wyk, "An overview of Integratable Current Sensor Technologies," *in Proc. 2003 Industry Applications Conference*, pp. 1251-1258.

[45] Z. Randjelovic, M. Kayal, R. Popovic, and H. Blanchard, "Highly Sensitive Hall Magnetic Sensor Microsystem in CMOS Technology," *IEEE Journal of Solid States*, Feb. 2002, pp. 151-159.

[46] A. Bilotii, G. Monreal, and R. Vig, "Monolithic magnetic Hall sensor using dynamic quadrature offset cancellation," *IEEE Journal of Solid States*, vol. 32, Jun. 1997, pp. 829-836.

[47] K. Nose and T. Sakurai, "Integrated Current Sensing Device for Micro IDDQ Test," *in Proc. 1998 test symposium*, pp. 323-326.

[48] Datasheet, "Current Sensor: ACS750xCA-050," Allegro Microsystems Inc., 2001.

[49] P. Midya, M. Greuel and P. Krein, "Sensorless Current Mode Control—An Observer Technique for DC-DC Converters", *IEEE Transactions on Power Electronics*, vol. 16, ul. 2001, pp. 522 –526.

[50] E. Dallago, M. Passoni, and G. Sassone, "Lossless current-sensing in low-voltage high-current DC-DC modular supplies," *IEEE Transactions on Industrial Electronics*, Dec. 2000, pp. 1249-1252.

Chapter 3

[51] H. P. Forghani-zadeh and G. A. Rincón-Mora, "Current-sensing techniques for DC-DC converters," in *Proc. 2002 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 577-580.

[52] E. Dallago, M. Passoni, and G. Sassone, “Lossless current-sensing in low-voltage high-current DC-DC modular supplies,” *IEEE Transactions on Industrial Electronics,* vol. 47, Dec. 2000, pp. 1249-1252.

[53] C. Enz and G. Temes, “Circuit techniques for reducing the effects of op-amp imperfections:-,” *IEEE Proceedings,* vol. 84, Nov. 1996, pp. 1584 -1614.

Chapter 4

[54] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[55] E. Dallago, M. Passoni, and G. Sassone, “Lossless current-sensing in low-voltage high-current DC-DC modular supplies,” *IEEE Transactions on Industrial Electronics*, Dec. 2000, pp. 1249-1252.

[56] *Coilcraft RF Inductors*. Coilcraft document 158, May 1999.

[57] *Coilcraft Power Inductors*. Coilcraft document 209-7, May 2000.

[58] K. Kundert, *Modeling the Skin Effect in Inductors*. Available from www.designersguide.com.

[59] L. Giacoletto, “Frequency- and time-domain analysis of skin effects,” *IEEE Transactions on Magnetics*, Jan. 1996, pp. 220-229.

[60] B. Oliver and J. Cage, *Electronic Measurements and Instrumentation.* New York, NY: McGraw Hill, 1971.

[61] K. Kantowitz, K. Kousourou, and G. Zucker, *Electronic Measurements.* Englewood, NJ: Prentice Hall, 1979.

[62] L. Schnell, *Technology of Electrical Measurements*. New York, NY: Wiley, 1993.

Chapter 5

[63] G. Rincon-Mora, "DC-DC converters: A topology journey, a tutorial," in *45th Midwest Symposium on Circuits and Systems (MWSCAS)*. Tulsa, OK, 2002.

[64] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[65] J. Kassakian, M. Schlecht, and G. Verghese, *Principles of Power Electronics*. New York, NY: Addison-Wesley, 1991.

[66] P. Krein, *Elements of Power Electronics*. New York, NY: Oxford University Press, 1998.

[67] R. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Transactions on Power Electronics*, vol 2, 1987, pp. 109-124.

[68] R. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Transactions on Power Electronics*, vol. 4, 1989, pp. 36-52.

[69] R. Ridley, "A new continuous-time model for current mode control," *IEEE Transactions on Power Electronics*, vol. 6, 1991, pp. 271-280.

[70] K. Yao, Y. Meng, and F. Lee, "Control bandwidth and transient response of buck converters," *in Proc. 2002 Power Electronics Specialist Conference*.

[71] K. Yao, Y. Meng, and F. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *IEEE Transactions on Power Electronics*, vol. 19, 2004, pp. 1454-1461.

[72] M. Brown, *Power Supply Cookbook*. Boston, MA: Newnes Publications, 1999.

Chapter 6

[73] H.P. Forghani-zadeh and G.A. Rincón-Mora, "A lossless, accurate, self-calibrating current-sensing technique for DC-DC converters," in *Proc. 2005 Industrial Electronics Conference (IECON)*, pp. 549 – 554.

[74] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE Journal of Solid States Circuits*, vol. 38, Mar. 2003, pp. 450-459.

[75] C. Enz and G. Temes, "Circuit techniques for reducing the effects of circuit imperfections," *Proceedings of IEEE,* Nov. 1996, pp. 1586-1614.

[76] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE Journal of Solid-State Circuits*, vol. 35, Dec. 2000, pp. 1877-1883.

[77] C. C. Enz, E. A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *IEEE Journal of Solid-State Circuits*, vol. SC-22, June 1987, pp. 335-342.

[78] C. G.Yu and R. L.Geiger, "Precision offset compensated op-amp with ping-pong control," *in Proc. 1992 Government Microcircuit Applications and Technology Conference (GOMAC)*, pp. 189-190.

[79] Y. Chong-Gun and R. Geiger, "An Automatic offset compensation scheme with ping-pong control for CMOS operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 29, May 1994, pp. 601-610.

[80] I. Opris and G. Kovacs, "A rail-to-rail ping-pong op-amp," *IEEE Journal of Solid-State Circuits*, Sept. 1996, pp. 1320-1324.

[81] M. C. Coln, "Chopper stabilization of MOS operational amplifiers using feed-forward techniques," *IEEE Journal of Solid-State Circuits*, vol. 16, Dec. 1981, pp. 745-748.

[82] I. G. Finvers, J. W.Haslett, and F. N. Trofimenkoff, "A high temperature precision amplifier," *IEEE Journal of Solid-State Circuits*, vol. 30, Feb. 1995, pp. 120-128.

[83] ICL7650S, *2MHz, Super Chopper-Stabilized Operational Amplifier*, Milpitas, CA: Intersil Corporation, Aug. 2005.

[84] MAX420, *±15V chopper-stabilized operational amplifier*, Milpitas, CA, Maxim Integrated Products Inc., Aug. 2005.

[85] H.P. Forghani-zadeh and G.A. Rincón-Mora, "A continuous, low-glitch, low-offset, programmable gain and bandwidth g_m-C filter," in *Proc. 2005 Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1629-1632.

[86] C. Toumazou, J. Lidgey, and D. Haigh, *Analogue IC Design: the Current-Mode Approach*, Peter Peregrinus Ltd: London, UK, 1990.

[87] K. Koli, *CMOS Current Amplifiers: Speed versus Nonlinearity*, PhD dissertation, Helsinki University of Technology, 2000.

[88] H. Elwan, A. Soliman, "Low-voltage low-power CMOS current conveyors," *IEEE Transactions on Circuits and Systems-I*, vol. 44, Sept. 1997, pp. 828-835.

[89] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York, NY: Wiley, 1997.

[90] R. Poujois and J. Borel, "A low-drift fully integrated operational amplifier," *IEEE Journal of Solid State Circuits*, vol. 13, Aug. 1978, pp. 499-505.

[91] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, NY: Wiley, 2001.

[92] C. Reis Filho and A. Santiago, "CMOS building blocks for smart-power integrated circuits," *in Proc. 1996 International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 892-896.

[93] B. Provost and E. Sanchez-Sinencio, "On-chip ramp generators for mixed-signal BIST and ADC self-test," *IEEE Journal of Solid State Circuits*, vol. 38, Feb 2003, pp. 263-273.

[94] J. Ramirez-Angulo, "A compact current controlled CMOS waveform generator," *Transactions on Circuits and Systems II*, vol. 39, Dec. 1992, pp. 883-885.

[95] L. Cheung and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid State Circuits*, vol. 39, Jan 2004, pp. 3-14.

[96] LM555 Datasheet, "LM555 timer," *National Semiconductor*, Feb. 2000.

[97] A. Sedra and K. Smith, *Microelectronic Circuits*. New York, NY: Oxford, 1998.

[98] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[99] R. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Transactions on Power Electronics*, vol. 4, Jan. 1989, pp. 36-52.

[100] P. Hazucha and et al., "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE Journal of Solid States Circuits*, vol. 40, Apr. 2005, pp**.** 838 – 845.

[101] P. Allen and D. Holberg, *CMOS Analog Circuit Design*. Oxford, NY: Oxford university press, 2002.

[102] R. Gregorian, *Introduction to CMOS Op- Amps and Comparators*. New York, NY: Wiley, 1999.

[103] C. Lee and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid States Circuits*, vol. 39, Jan. 2004, pp. 3-14.

[104] G. Rincon-mora, "DC-DC converters: a topology journey," tutorial presented at *45th Midwest Symposium on Circuits and Systems (MWSCAS),* Aug. 2002

[105] B. Razavi, *Design of Analog Integrated Circuits*. New York, NY: McGraw Hill, 2001.

[106] A. Hastings, *The Art of Analog Layout*. New York, NY: Prentice Hall, 2000.

Chapter 7

[107] *XYZ's of Oscilloscopes,* Tektronix LLC: Richardson, TX, www.tektroniks.com.

[108] *ABC's of Probes,* Tektronix LLC: Richardson, TX, www.tektroniks.com.

[109] *TDS 420A Digitizing Oscilloscopes Instruction Manual,* Tektronix LLC: Richardson, TX, www.tektroniks.com.

Chapter 8

[110] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proc. 2004 Power Semiconductor Devices and ICs*, pp. 13-21.

[111] B. Miao, R. Zane, and D. Maksimovic, "System identification of power converters with digital control through cross-correlation methods," *IEEE Transactions on Power Electronics,* vol. 20, Sept. 2005, pp. 1093- 1099.

[112] C. Lee and P. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid-State Circuits*, vol. 39, Jan. 2004, pp. 3-14.

[113] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE Journal of Solid-State Circuits*, vol. 38, Mar. 2003, pp. 450-459.

[114] E. Dallago, M. Passoni, and G. Sassone, "Lossless current-sensing in low-voltage high-current DC-DC modular supplies," *IEEE Transactions on Industrial Electronics*, vol. 47, Dec. 2000, pp. 1249-1252.

[115] N.A. Keskar and G.A. Rincón-Mora, "Self-stabilizing, integrated, hysteretic boost DC-DC converter," in *Proc. 2004 IEEE Industrial Electronics Conference (IECON),* pp. TA3-4.

[116] G. Rincón-Mora, *Power Management ICs - A Top-Down Design Approach.* Rincon-Mora, Atlanta: Georgia, 2005.

[117] Current-sharing techniques for VRMs, *Technical Brief TB385.1*, Milpitas, CA: Intersil Corporation.

[118] W. Ki, D. Ma, "Single-inductor multiple-output switching converters," *in Proc. 2001 IEEE Power Electronics Specialists Conference (PESC)*, pp. 226 – 231.

[119] L.A. Milner and G.A. Rincón-Mora, "A novel predictive inductor multiplier for integrated circuit dc-dc converters in portable applications," in *Proc. 2005 International Symposium on Low Power Electronics and Design (ISLPED).*

[120] B. Boser, "Digitally assisted analog circuits," *Presented in EECS Joint Colloquium Distinguished Lecture Series University of California, Berkeley*, [online document], 2004, [cited 2006, Apr. 1], Available HTTP: *http://www.eecs.berkeley.edu/~boser/presentations/2004-05-18%20TSMC.pdf*

[121] B. Murmann and B. Boser, *Digitally Assisted Pipelined ADCs.* Boston, MA: Kluwer, 2004.

[122] P. Hasler and D. Anderson**, "**Cooperative analog-digital signal processing," *in Proc. 2002 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, pp. 3972-3975.

[123] R. Rutenbar, "Future of IC design in 2010," MACRO center for circuits and system solutions, 2004.

Appendix A

[124] G. Gielen and R. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proceedings of the IEEE*, vol. 88, Dec. 2000, pp. 1825-1854.

[125] E. Acuna, J. Dervenis, A. Pagones, F. Yang, and R. Saleh, "Simulation techniques for mixed analog/digital circuits," *IEEE Journal of Solid State Circuits*, vol. 25, April 1990, pp. 353-363.

[126] R. Saleh, B. Antao, and J. Singh, "Multilevel and mixed-domain simulation of analog circuits and systems," *IEEE Transactions on Computer Aided Design*, vol. 15, Jan. 1996, pp. 68-82.

[127] K. Kundert, H. Chang, D. Jefferies, G. Lamant, E. Malavasi, and F. Sendig, "Design of mixed-signal systems-on-a-chip," *IEEE Transactions on Computer-Aided Design*, vol. 19, pp. 1561-1571, Dec. 2000.

[128] K. Kundert, "A formal top-down design process for mixed-signal circuits," *in proc. 2000 workshop on advances in analog circuit design*.

[129] P. Miliozzi, K. Kundert, K. Lampaert, P. Good, and M. Chian, "A design system for RFIC: challenges and solutions," *Proceedings of the IEEE*, vol. 88, Oct. 2000, pp. 1613 – 1632.

[130] K. Kundert, "Future directions in mixed-signal behavioral modeling," *in proc. 2002 IEEE Workshop on Behavioral Modeling and Simulation*, pp. 150 – 183.

[131] K. Kundert and I. Clifford, "Achieving accurate results with a circuit," *in proc. 1993 IEE Colloquium on SPICE: Surviving Problems in Circuit Evaluation*, pp. 4/1 - 4/5.

[132] M. McCorquodal et al., “A top-down mirosystems design methodology and associated challenges,” *in proc. 2003 Design, Automation, and Test in Europe Conference*, pp. 1530-1534.

[133] F. Guinjoan, J. Calvente, A. Poveda, and L. Martinez, “Large signal modeling and simulation of switchnig dc-dc converters,” *IEEE Trans. Power Electron.*, vol. 12, Dec. 1997, pp. 485-495.

[134] Y. S.Lee, D. K. W.Cheng, and S. C. Wong, “A new approach to the modeling of converters for SPICE simulation,” *IEEE Trans. Power Electron.*, vol. 7, pp. 741-753, Oct. 1992.

[135] I. Zafrany and S. Ben-Yaakov, “Average modeling, analysis and simulation of current shared DC-DC converters,” *in proc. 1998 IEEE Power Electronics Specialist Conference*, pp. 640 – 646.

[136] F. Leung, T. Ng, and P. Tam, “A CAD package for fast simulation of regulated DC-DC converters in large-signal,” *in proc. 1997 IEEE Industrial Electronics Conference*, pp. 755 – 758.

[137] A. Consoli, S. Baglio, L. Fortuna, S. Sueri, and D. Tagliavia, “Modeling and simulation of a current programmed DC-DC converter: a new strategy,” *in proc. 1991 International Symposium on Circuits and Systems (ISCAS)*, pp. 2256 – 2259.

[138] K. Kundert and J. White, “Efficient simulation of switching power circuits,” *in proc. 1988 IEEE Workshop on Computers in Power Electronics*, pp. 23 – 27.

[139] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[140] P. Krein, *Elements of Power Electronics*. New York, NY: Oxford University Press, 1998.

[141] K. Kundert, *The Designer’s Guide to Spice and Spectre*. Boston, MA: Springer, 1995.

[142] Accelera, *Verilog-AMS Language Reference Manual*, Accelera Standard, Nov. 2004. MA: Springer, 2004.

[143] K. Kundert and O. Zinke, *The Designer Guide to Verilog AMS*. Boston, MA: Springer, 2003.

[144] P. Allen and D. Holberg, *CMOS Analog Circuit Design*, New York, NY: Oxford, 2002.

[145] William J. McCalla, *Fundamentals of Computer-Aided Circuit Simulation*. Boston, MA: Kluwer Academic Publishers, 1993.

Appendix B

[146] M. Gildersleeve, H.P. Forghani-zadeh, and G.A. Rincon-Mora, **"**A comprehensive analysis and a highly efficient, mode-hopping DC-DC converter," in *Proc. 2002 Asian-Pacific Conference on ASICs*, pp. 153-156.

[147] G.A. Rincon-mora, "DC-DC converters: a topology journey," *tutorial presented n 45th Midwest Symposium on Circuits and Systems (MWSCAS)*, Tulsa, OK, Aug. 2002.

[148] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Norwell, MA: Kluwer Academic Publishers, 1999.

[149] J. Kassakian, M. Schlecht, G. Verghese, *Principles of Power Electronics*, New York, NY: Addison-Wesley, 1991.

[150] P. Krein, *Elements of Power Electronics*, New York, NY: Oxford University Press, 1998.

[151] M. Brown, *Power Supply Cookbook*, Boston, MA: Newnes Publications, 1999.

[152] Chrysis, *High Frequency Switching Power Supplies*, New York, NY: McGraw-Hill, 1989.

[153] J. Lenk, *Simplified Design of Switching Power Supplies*, Boston, MA: Butterworth-heinemann, 1995.

[154] S. Maniktala, "SIMPLE SWITHCER® PCB layout guidelines," National Semiconductor Corporation, Santa Clara, CA, Application Note 1229, 2002.

[155] C. Jensen, “Layout guidelines for switching power supplies,” National Semiconductor Corporation, Santa Clara, CA, Application Note 1149, 1999.

[156] “Layout considerations for non-isolated DC-DC converters,” Maxim IC, Sunnyvale, CA, Application Note APP735, March 2001.

[157] “PCB design guidelines for reduced EMI,” Texas Instruments, Dallas, TX, Application Note SZZA009, Nov. 1999.

[158] “EL7554: Monolithic 4Amp DC-DC step-down regulator,” Intersil, Milpitas, CA, Datasheet FN7360, Aug. 2003.

[159] “LTC3429: 600mA, 500KHz micro-power synchronous boost converter with output disconnect,” Linear Technology, Milpitas, CA, Datasheet 3429F, 2003.

[160] ADP3050: 200KHz, 1A high-voltage step-down switching regulator,” Analog Devices, Norwood, MA, Datasheet ADP3050_a, 2000.

[161] “FAN5307: High-efficiency step-down DC-DC converter,” Fairchild semiconductor, South Portland, ME, Datasheet FAN5307, Dec. 2003.

[162] E.B. Rosa, “The self and mutual inductance of linear conductors,” *Bulletin of the Bureau of Standards*, Vol. 4, 1908, pp. 301-303.

[163] Alan Hastings, *The Art of Analog Layout,* New York, NY: Prentice Hall, 2000.

[164] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, New York, NY: IEEE Press, 1996.

[165] T. Hubing, “PCB EMC design guidelines: a brief annotated list,” in *Proc. International symposium on Electromagnetic Compliancy*, Aug. 2003, pp. 34-36.

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